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Ku-Band Field-Effect Power Transistors

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16. Abstract

This report describes the work performed during a 20-month research program to develop GaAs FETs and associated circuitry for medium-power Ku-band amplifiers. The program design goals are to obtain an output power of 2W over the 13- to 15.5-GHz band with a power gain of 6 dB and power-added efficiency of 25%. The program comprises materials research, device technology development, and amplifier studies.

The major materials effort in this program was the growth of n^+-n-SI GaAs wafers for the device development effort. Device quality epitaxial material was produced by three $AsH_3/Ga/HCl/H_2$ (hydride) reactors and one $AsCl_3$ reactor. The technology of growing Cr-doped buffer layers in the hydride system was refined to achieve excellent surface morphology. The voltage breakdown of Cr-doped layers was in excess of 1500 V with resistivity of the order of 10^7 ohm-cm. Undoped buffer layers grown with the two-bubbler $AsCl_3$ system had resistivities of about 10^5 ohm-cm. Device quality n-SI GaAs wafers were also produced by ion implantation in the 50- to 250-keV energy range using ^{28}Si ions. A method of annealing ion-implanted wafers without encapsulation was developed to achieve excellent surface morphology.

Devices were produced by two fabrication techniques. The bulk of the devices was fabricated by a previously developed self-aligned gate process. During the project an aligned-gate fabrication process was developed. A novel feature of this process is the use of a moat etch plus anodic thinning to compensate for epitaxial layer thickness variations by automatically thinning the gate channels to the pinch-off thickness while leaving a layer of n^+ material in the source and drain regions. A double layer photoresist technique was developed to allow clean lift-off of thick gate metallization. The key features of our FET device technology are: (a) use of refactory, Au-based metallization for the source, drain, and gate contacts, and (b) flip-chip mounting. The highest output power at 15 GHz achieved in this program was 1.05 W. The best efficiency at 15 GHz was 19% with 0.74-W output power. Preliminary accelerated life test data on RCA FETs indicates an MTBF of at least 1.4×10^6 h, based on a conservative estimate of 1-eV activation energy and 130°C channel temperature.

In this project a single-stage amplifier was developed using an 8-gate, 1200-μm width device to give a gain of 3.3 ± 0.1 dB over the 14.4- to 15.4-GHz band with an output power of 0.48 W and 15% minimum efficiency with 0.255 W of input power. With two 8-gate devices combined and matched on the device carrier, using a newly developed lumped-element format, a gain of 3 dB was attained over the 14.5- to 15.5-GHz band with a maximum efficiency of 9.9% for an output power of 0.8 W.

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PREFACE

This final report describes research carried out at the Microwave Technology Center of RCA Laboratories during the period 9 November 1977 to 8 August 1979 in a program sponsored by Goddard Space Flight Center under Contract No. NAS5-24355. F. Sterzer is the Center's Director and S. Y. Narayan is the Project Supervisor.

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SECTION I

INTRODUCTION

The objective of this 20-month program is to advance the state-of-the-art of GaAs power field-effect-transistor (FET) technology to develop GaAs FETs and associated circuitry for medium-power Ku-band amplifiers. The program design goals are to obtain an output power of 2 W over the 13- to 15.5-GHz band with a power gain of 6 dB and power-added efficiency of 25%.

Table 1 summarizes the best results obtained from RCA's GaAs power FETs produced during this report period. The highest output power at 15 GHz achieved in this program was 1.05 W from wafer D147. The best efficiency at 15 GHz was 19% with 0.74-W output power from wafer C182.

The key features of our FET device technology are: (a) use of refractory, Au-based metallization for the source, drain, and gate contacts and (b) flip-chip mounting. The use of refractory Au-based metallization, particularly for the Schottky-barrier gate contact, results in higher device reliability. Unlike low-noise FETs, power FETs operate at high channel temperature, large rf voltage swings, and high rf gate current in both the forward conduction and reverse breakdown regions. These factors enhance intermetallic diffusion and electromigration, which are common failure modes. Intermetallic diffusion and electromigration are strongly dependent on the gate metallization and are particularly severe for Al-based gates. The operating-channel temperature depends substantially on the design and packaging of the FET. The flip-chip mounted design pioneered by RCA under USAF Avionics Laboratory sponsorship (Contract No. F33615-73-C-1042) leads to both low thermal resistance and low parasitic source inductance. Measurements show that the temperature rise in a flip-chip bonded FET capable of 1 W of rf output is only about 60 to 65°C. As a result of these two factors, RCA power FETs have potential for high reliability. Preliminary accelerated life test data on RCA FETs indicate an MTBF* of at least 1.4×10^6 h, based on a conservative estimate of 1-eV activation energy and 130°C channel temperature.

*MTBF = mean time before failure.

TABLE 1. SUMMARY OF GaAs POWER FET PERFORMANCE

Wafer No.	FET Type	Frequency (GHz)	Power Gain (dB)	Output Power (W)	Power-Added Efficiency (%)
A105	18 Gate	10	3.9	1.26	11.8
C182	8 Gate	15	3.1	0.743	19
B995	18 Gate	15	1.5	0.556	3.8
D147	18 Gate	15	2.0	1.05	8.6
D169	8 Gate	10	4.4	0.476	11.5
D319	18 Gate	15	2.14	0.88	6.7
C521	8 Gate	15	3.2	0.66	10.7
20392-C	8 Gate	15	3.5	0.41	14.6

In this study we have developed a single-stage amplifier, using an 8-gate 1200-μm-width device, which demonstrated a gain of 3.3 $\pm$0.1 dB over the 14.4- to 15.4-GHz band with an output power of 0.48 W and 15% minimum efficiency with 0.255 W of input power. With two 8-gate devices combined and matched on the device carriers, using a newly developed lumped-element format, a gain of 3 dB was achieved over the 14.5- to 15.5-GHz band with a best efficiency of 9.9% and an output power of 0.8 W.

This report describes in detail our research effort in the material technology, FET design and fabrication techniques, and amplifier development.

SECTION II

MATERIALS RESEARCH ON GaAs EPITAXY

A. INTRODUCTION

The objective of the materials research part of this program is to improve the quality of epitaxial n-GaAs used for FET fabrication. GaAs power FETs require submicrometer thicknesses of n-GaAs grown on semi-insulating (SI) GaAs substrates. Since the current in the power FET flows through this submicrometer-thick n-layer in close proximity to the SI substrate, it is essential to control the quality of the n-layer substrate interface. Furthermore, gate lengths on the order of 0.75 to 1.0 μm have to be defined during device fabrication. We are currently using conventional optical lithography to achieve such gate lengths. The use of optical lithography puts very stringent requirements on the surface morphology of the epitaxial layers. Blemishes of submicrometer dimensions cannot be tolerated. As discussed later, it is also necessary to ensure that the GaAs substrate used be extremely flat; a very slight convexity can be tolerated during photolithography, but any concavity prevents achievement of micrometer resolution. These stringent constraints make epitaxy for GaAs FETs a very challenging task. In addition to carrying out research on epitaxy, a large number of wafers have to be supplied for device development. This section describes the work performed during this phase of the program, including our achievements and problem areas.

B. GaAs EPITAXY

The FET active layers were grown using vapor-phase epitaxy (VPE). Both the hydride ($AsH_3/HCl/Ga/H_2$) and trichloride ($AsCl_3/Ga/H_2$) systems were employed. Table 2 summarizes the characteristics of the four GaAs reactors which were used. At program start, only the hydride reactors A and B were operational. A third hydride system, reactor C, became operational in May 1977. A two-bubbler $AsCl_3$ system, reactor D, became operational in November 1977. These reactors were designed, fabricated, and debugged under company sponsorship.

TABLE 2. GaAs VAPOR-PHASE EPITAXIAL REACTORS

Reactor No.	Reactor Type	Tube Diameter (cm)	Doping Capability	Comments
A	$Ga/AsH_3/Cl_2/H_2$ (Hydride System)	2.5	S, Si for n-type; Cr for high ρ buffers	Used for developing technology for the growth of Cr-doped, high-resistivity buffer layers.
B	$Ga/AsH_3/Cl_2/H_2$ (Hydride System)	5	S, Si for n-type	Capability for growth of large-diameter wafers.
C	$Ga/AsH_3/Cl_2/H_2$ (Hydride System)	2.5	S, Si for n-type	Newly built and completely operational. Has improved gas handling system which incorporates the experience gained in A and B reactors.
D	$Ga/AsCl_3/H_2$ (Trichloride System)	5	S, Si for n-type	Two-bubbler $AsCl_3$ system. $AsCl_3$ mole fraction can be varied for growth of undoped buffer layers.

1. Hydride Reactor Systems

The basic details of our $AsH_3/Ga/HCl/H_2$ reactors are well known and described in the literature [1]. Ga is transported as GaCl by the reaction of HCl gas with the source Ga. GaCl reacts with As_2 and As_4 formed by the dissociation of AsH_3 and forms GaAs which deposits on a substrate. The source materials, namely, Ga, AsH_3, and HCl, are selected so that the background doping is in the 10^{14} cm^3 range. N-layers are grown by either doping with S introduced as gaseous H_2S or Si introduced as SiH_4. All gas lines are filtered, and gas flows are electronically controlled with commercial mass flow controllers.

1. S. T. Jolly, L. C. Upadhyayula, H. C. Huang, and B. J. Levin, "Junction Growth Techniques for GaAs Avalanche Transit-Time Devices," U.S. Army Electronics Command, Fort Monmouth, New Jersey, ECOM-0308-F, 1973.

The typical power FET wafer is a multilayer structure composed of a 1-μm-thick active n-layer doped to 8 to 10×10^{16} cm^{-3}. A 0.5-μm-thick n^+-layer is grown on the n-layer and doped to 5×10^{18} cm^{-3} for the source and drain ohmic contacts. These layers are grown in situ to ensure a good n^+-n interface. Sometimes a buffer layer is grown between the n-layer and the SI substrate to isolate the active layer from the bulk-grown substrate.

One of the major problems currently facing epitaxy for GaAs FETs is the inconsistency in the quality of the commercially available bulk-grown SI GaAs substrate. The problem of poor and/or inconsistent substrate quality can be solved by using the well-known concept of the epitaxial "buffer" layer. The problem with buffer layers for GaAs FETs is that a high resistivity ($\rho \geq 10^5$ ohm-cm) epi-layer is required. The state-of-the-art of the growth of such buffer layers is still in its infancy. We have demonstrated the feasibility of the growth of chromium-doped epitaxial buffer layers. FETs with 1.5-μm gate length fabricated from wafers with such buffer layers have operated at frequencies as high as 22 GHz [2]. There are still many problems with the epi-growth of chromium-doped layers which remain to be solved.

Figure 1 is a schematic diagram of the gas-handling system for the hydride reactor modified for the growth of epitaxial SI GaAs layers. This reactor has the following characteristics:

(1) Ability to operate as a "normal" Ga/HCl/AsH_3 system employing palladium-diffused hydrogen as the diluting gas. It is also planned to add the ability to substitute ultrapure nitrogen for the hydrogen. This will be of significance in attempts to employ metallic chromium or iron as the doping element.

(2) A third input line was added to the reactor to allow the introduction of chromyl chloride/helium mixture of variable composition.

(3) An HCl feed was added to the arsine/hydrogen line to allow a mixture of hydrogen chloride to the reactant gases downstream of the gallium boat to determine the effect of HCl partial pressure on growth rate, background carrier concentration, etc. This HCl was also used to etch clean the reactor tube and substrate holder prior to the deposition runs.

2. H. C. Huang, I. Drukier, R. L. Camisa, S. T. Jolly, J. Goel, and S. Y. Narayan, "GaAs MESFET Performance," IEDM Digest, Washington, DC, December 1975, pp 235-237.

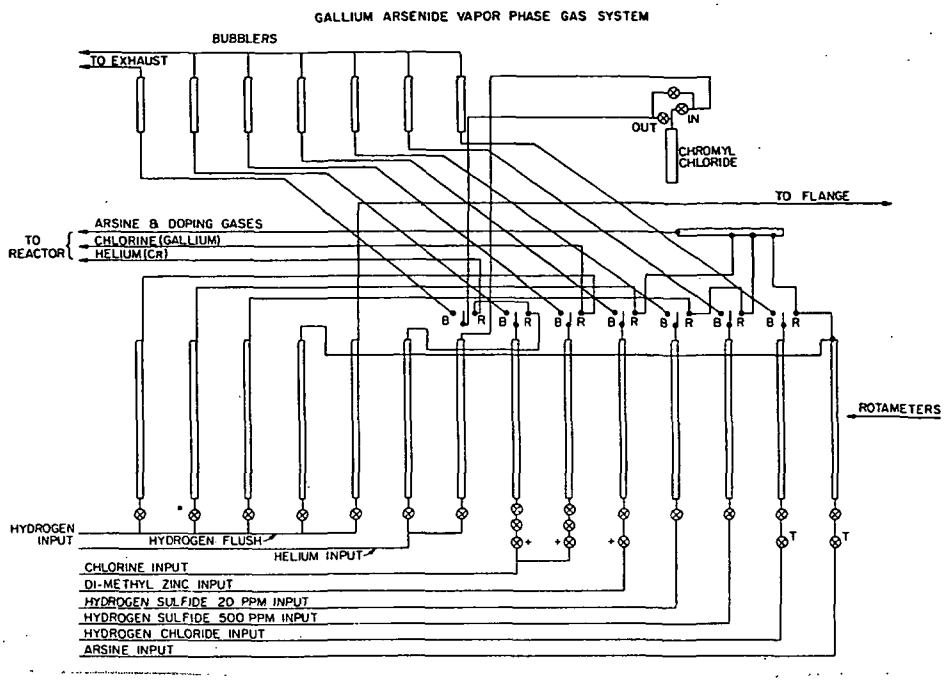


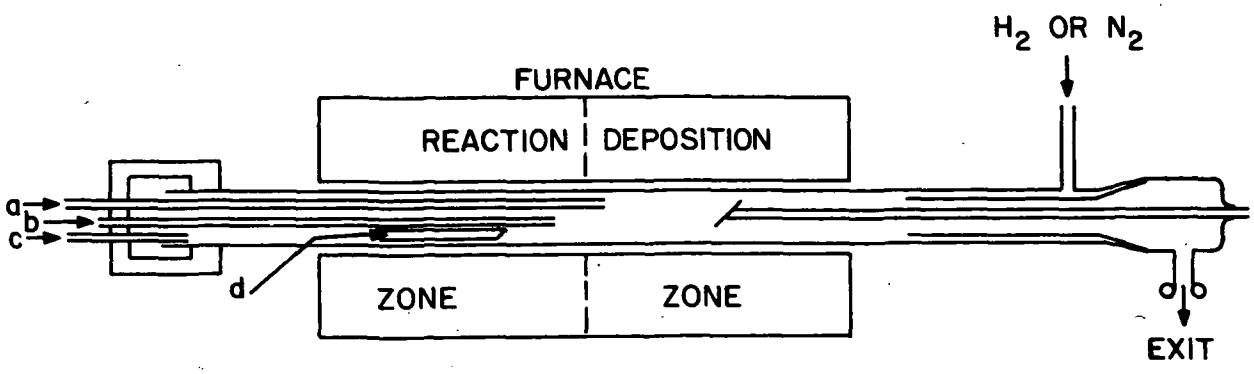
Figure 1. Schematic diagram of reactor gas-handling system.

(4) n-type doping gases such as hydrogen sulfide, hydrogen selenide, or hydrogen telluride could be introduced.

(5) Inclusion of a line for addition of other doping materials such as diethylzinc to allow p-type doping.

(6) An ability to introduce chlorine into the chromium doping line. The use of metallic chromium or iron in the chromium feed tube of the reactor permits the addition of the respective metallic chlorides into the reacting gas stream. This could be a considerably safer and more convenient method of adding chromium than the use of chromyl chloride.

Figure 2 is a schematic diagram of the reactor tube and furnace assembly. The reactor tube configuration has been changed from that previously employed at RCA for vapor deposition of GaAs by the $Ga/HCl/AsH_3$ system. The sidearm previously used to discharge the waste products of the system has been eliminated.



a CHROME TUBE
b AsH_3 TUBE
c Cl_2 OR HCl TUBE
d GALLIUM BOAT

Figure 2. Schematic diagram of reactor tube/furnace assembly.

The reactor now consists of a single straight quartz tube. The exit end of the tube is closed by an end cap with a sleeve extending so far up the reactor tube that sliding the furnace down the tube permits it to be heated and etched clean of reaction products. A small quantity of hydrogen or nitrogen flows slowly upstream between the reactor tube and the sleeve; this restricts reaction products to the interior of the sleeve and prevents their deposition on the walls of the reactor tube downstream of the end of the sleeve. The substrate holder is incorporated in the end-cap holder-sleeve assembly and extends beyond the end of the sleeve into the deposition region of the reactor.

The elimination of the sidearm achieves several objectives:

(1) It eliminates the necessity to dismantle the assembly to remove the reactor tube for cleaning whenever the performance of the reactor is affected by the deposits of reaction products in a sidearm.

(2) It reduces the history effect (i.e., change in the background impurity level produced after growth of highly doped layers). This feature is important when attempting to grow a buffer layer after a highly doped device wafer has been grown.

(3) The reactor tube can be etch-cleaned (with hydrogen chloride gas) before every run without dismantling the system.

(4) The gas flow pattern is uniform down to the tube and is not affected by the reverse gas flow from the loading end of the reactor, required to force the reaction products down the side exit arm.

Other features of the reactor assembly are the use of a sapphire feed tube for the introduction of the chromyl chloride/helium mixture into the reaction zone and the use of a pyrolytic boron nitride sleeve to protect the reactor tube from attack by the chromyl chloride in the reaction zone.

The surface morphology of Cr-doped layers grown in the modified reactor is excellent. This is in contrast to the layers grown in our older reactor. Possible explanations for this are the complete cleaning of the reactor with HCl prior to growing and the elimination of the sliding substrate feed rod.

2. Trichloride System

The two-bubbler trichloride reactor is similar to that described in the literature [3]. The trichloride system requires only two high purity components (in addition to H_2), namely, $AsCl_3$ and Ga. This is in contrast to the hydride system wherein Ga, AsH_3, and Cl_2 (or HCl) are required. Further, higher purity $AsCl_3$ than AsH_3 can be commercially obtained. Another advantage of the trichloride system is that the background doping can be changed by varying the $AsCl_3$ mole fraction [3].

The trichloride system can be used to grown "undoped" buffer layers by using a flow of "bypass" $AsCl_3$. This flow bypasses the Ga region and enters the reaction region. The bypass flow results in higher HCl present in the deposition zone and causes the background doping to fall to the 10^{12} cm^{-3} region [3].

Figure 3 is a plot of (N_D-N_A) as a function of the $AsCl_3$ mole fraction for our trichloride reactor. All these results are for layers grown on bulk-grown SI GaAs substrates. Note that (N_D-N_A) in the mid-10^{14} cm^{-3} region can be grown.

3. H. M. Cox and J. V. DiLorenzo, "Characteristics of an $AsCl_3/Ga/H_2$ Two Bubbler GaAs CVD System for MESFET Application," Proc. of the Sixth International Symp. on GaAs and Related Compounds; Int. of Phys., Conf. Series, No. 336, London, 1977, pp. 11-22.

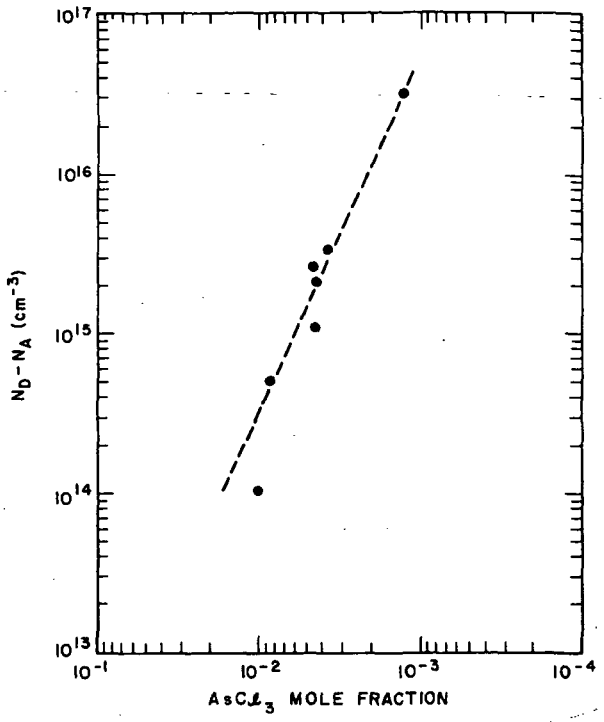


Figure 3. N_D-N_A as a function of $AsCl_3$ mole fraction for RCA $AsCl_3/Ga/H_2$ reactor.

C. EXPERIMENTAL RESULTS

1. Epitaxial Growth of Cr-Doped Layers

In the early part of this program phase, the effort on epitaxial growth of Cr-doped layers in reactor A [4] using CrO_2Cl_2 as the doping gas was continued. Figure 4 shows a two-point probe I-V characteristic of wafer A447. This wafer has a 5-μm-thick epitaxial layer grown on a SI GaAs substrate. The leakage current in the dark was about 2 μA at 1400 V. The top trace shows the increase in current when the sample is illuminated by a microscope lamp. Figure 5 shows similar traces for run A448. Figure 5(a) shows the dark and illuminated characteristic for the starting substrate while Fig. 5(b) shows similar traces after the growth of 11 μm of Cr-doped epitaxial layer.

4. S. T. Jolly et al., Epitaxial Growth of Semi-Insulating GaAs, Annual Report, Contract N00014-77-C-0542, DARPA Order No. 3461, Basic Program Code 7D10, March 1978.

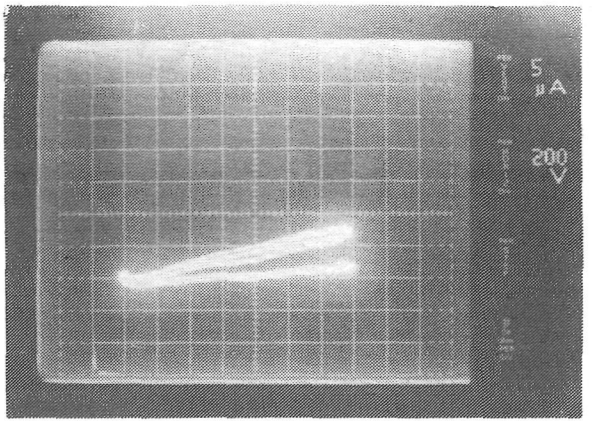


Figure 4. Two-point probe I-V characteristic of wafer A447.

Several thin n-type layers were grown on top of Cr-doped epitaxial buffer layers. These layers were grown in situ. Some examples are listed in Table 3.

Figures 6 and 7 show the carrier concentration profiles of wafers A436 and A437, respectively, as measured by an automatic impurity profiler. Figures 8 and 9 show carrier profiles of A441 and A443 deduced from a conductivity profile assuming an average mobility.

Attempts to grow n^+ layers on Cr-doped epitaxial layers were unsuccessful. The grown layers showed an anomalous diffusion of the n^+-dopant. It was suggested* that this anomalous diffusion was due to lattice damage due to excessive Cr concentration. Attempts to measure Cr concentration in epitaxial buffer layers have been unsuccessful to date. Based on these results, it was decided to attempt to reduce the background carrier concentration in the reactor so that less Cr will be required to trap the carriers and render the layer semi-insulating. It was therefore decided to implement a new reactor design.

2. Reactor B

It was decided to design, fabricate, and make operational a reactor system utilizing the Crystal Specialties** gas control system, using a reactor tube and furnace assembly capable of processing a large wafer. The first task was to reduce the background carrier concentration in the reactor.

*M. N. Yoder, ONR, Private Communication.
**Crystal Specialties, Inc., Monrovia, CA.

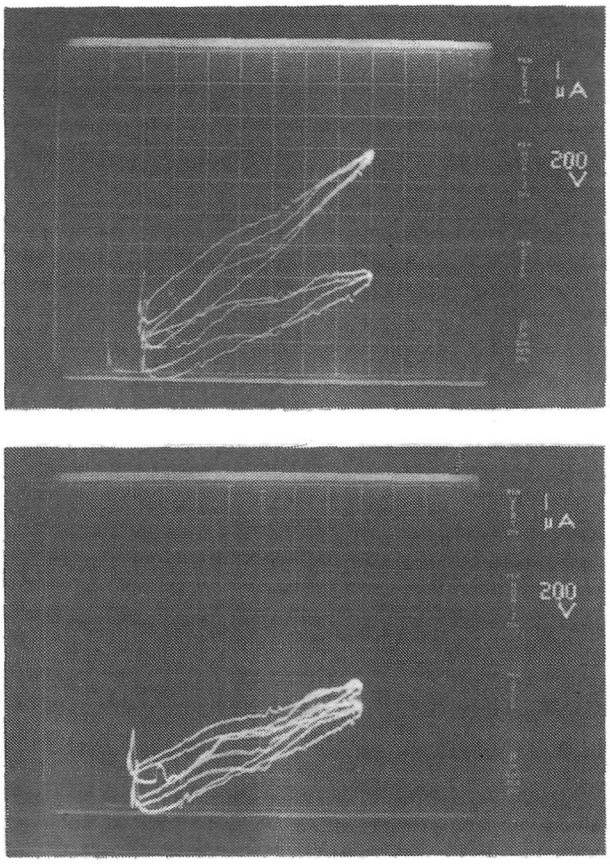


Figure 5. (a) Dark and illuminated two-point probe I-V characteristic of starting substrate. (Nikkei Kako 4418). (b) Similar characteristics of Cr-doped epitaxial layer A448.

TABLE 3. WAFERS WITH EPITAXIAL BUFFER LAYERS

Parameter	A436	A437	A441	A442
Buffer Thickness (μm)	6.5	6.0	6.0	6.0
Active Layer (μm)	1	1	1.5	1.5
Carrier Concentration (cm^{-3})	$3x10^{16}$	$1.5x10^{16}$	$4x10^{16}$	$1x10^{17}$
Room Temp Mobility	5745	6284	Not checked	Not checked
77 K ($cm^2V^{-1}s^{-1}$)	12820	15435	Not checked	Not checked

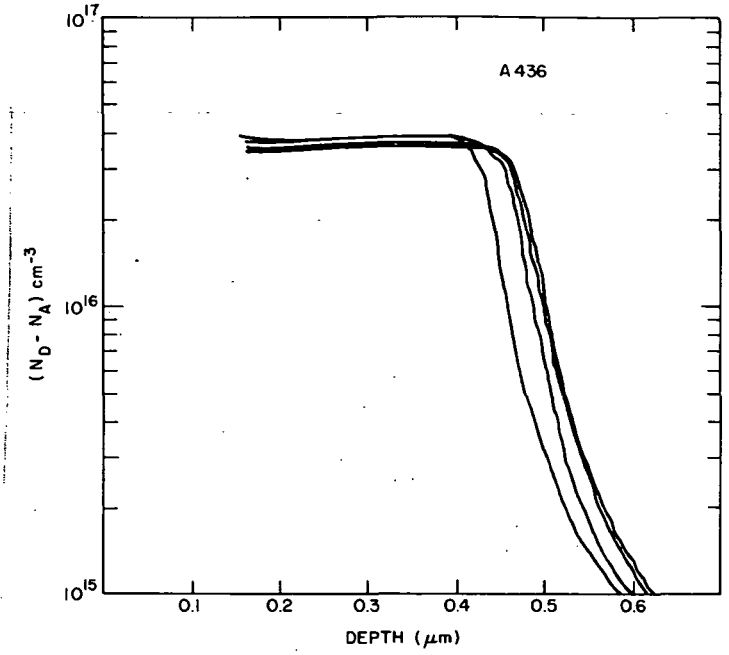


Figure 6. Carrier profile of n-layer grown on Cr-doped epitaxial buffer layer. Run A436.

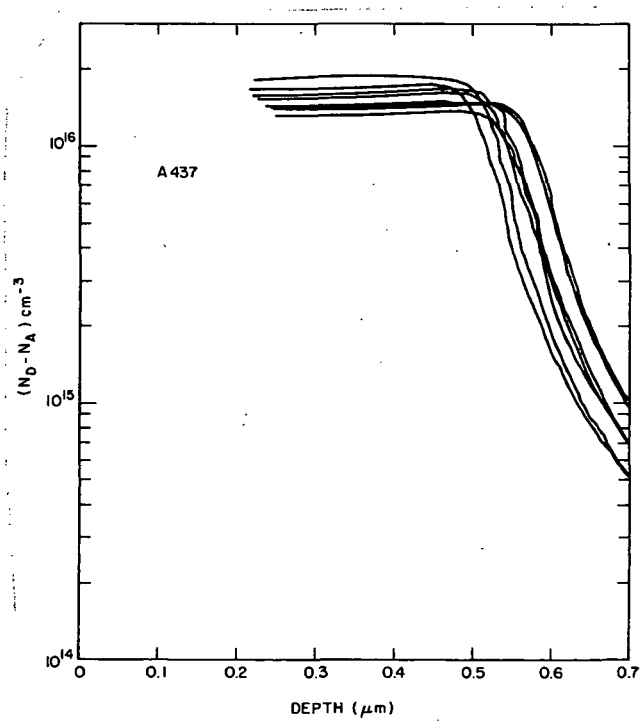


Figure 7. Carrier profile of n-layer grown on Cr-doped epitaxial buffer. Wafer A437.

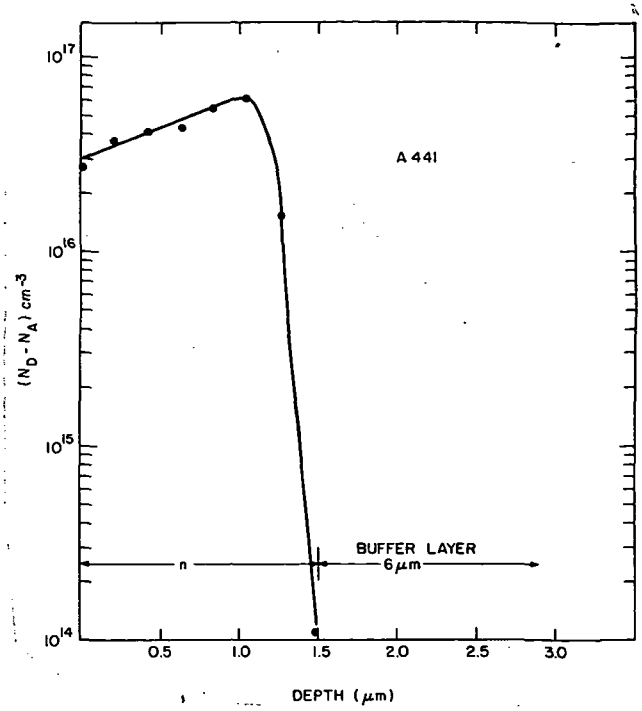


Figure 8. Carrier profile of A441 deduced from conductivity measurements assuming constant mobility.

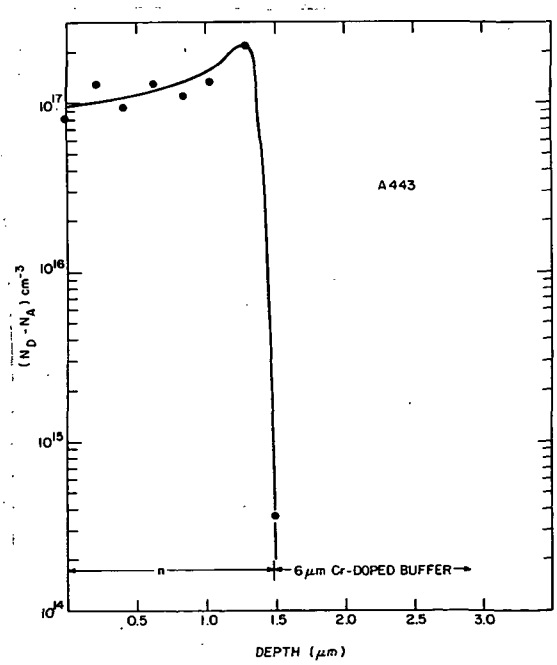


Figure 9. Carrier profile of A443 deduced from conductivity measurements assuming constant mobility.

a. Gettering of Si Using NH_3

A major source of residual donors in GaAs wafers grown in a quartz reactor tube is silicon. It has been reported that the addition of NH_3 to the gas stream removes Si in the form of Si_3N_4 and prevents incorporation of Si in GaAs [5]. Under normal operating conditions, the background carrier concentration obtained in reactor B is $2\text{-}3\times10^{15}$ cm^{-3}. By introducing NH_3 into the gas stream, n-layers with carrier concentration on the order of 10^{13} cm^{-3} and lower have been grown. By increasing the partial pressure of NH_3, even p-type layers have been grown. Equipment using very high impedance electrometers is being developed to allow van der Pauw measurements on these high-resistivity layers. We have grown high-resistivity layers 6 to 8 μm in thickness; this is about twice the thickness reported in the literature [5]. Figure 10 shows the two-point probe I-V characteristic of two such layers.

The effect of the NH_3 'doped' buffer layer can be seen by the comparison of results obtained in runs B176 and B179. Run B176 is a 3.9-μm undoped layer grown on 5.5-μm-thick NH_3 'doped' buffer layer. Run B179 is a 5.5-μm-thick undoped layer. The top 2.5 μm of B179 is an n-layer of the same carrier concentration (3×10^{15} cm^{-3}) as the n-layer in B176 and the bottom 3 μm is a high-resistivity layer ('undoped buffer') due to diffusion of acceptors from the SI GaAs substrate. Table 4 shows the result of a van der Pauw measurement. Figures 11 and 12 show the doping profile of these wafers. A small number of TELD and FET wafers have been grown for evaluation.

b. Effect of Carrier Gas Flow Rate

The background doping in reactor B as a function of the carrier gas flow has been investigated [6]. It has been possible to reduce the carrier concentration by reducing the flow rate of the diluent H_2 in the reactor without changing the flow rates of the active gases, viz., AsH_3 and HCl. Figure 13 shows the carrier concentration as a function of the flow rate. Wafer B287 had a thin (3.8 μm) layer which could not be profiled since the depletion

5. G. B. Stringfellow and G. Horn, "Hydride VPE Growth of GaAs for FETs," J. Electrochem. Soc. 134, 1806 (1977).
6. J. K. Kennedy et al., "Effect of H_2 Carrier Gas Flow Rate on the Electrical Properties of GaAs in a Hydride System," J. Crystal Growth 24/25, 233 (1974).

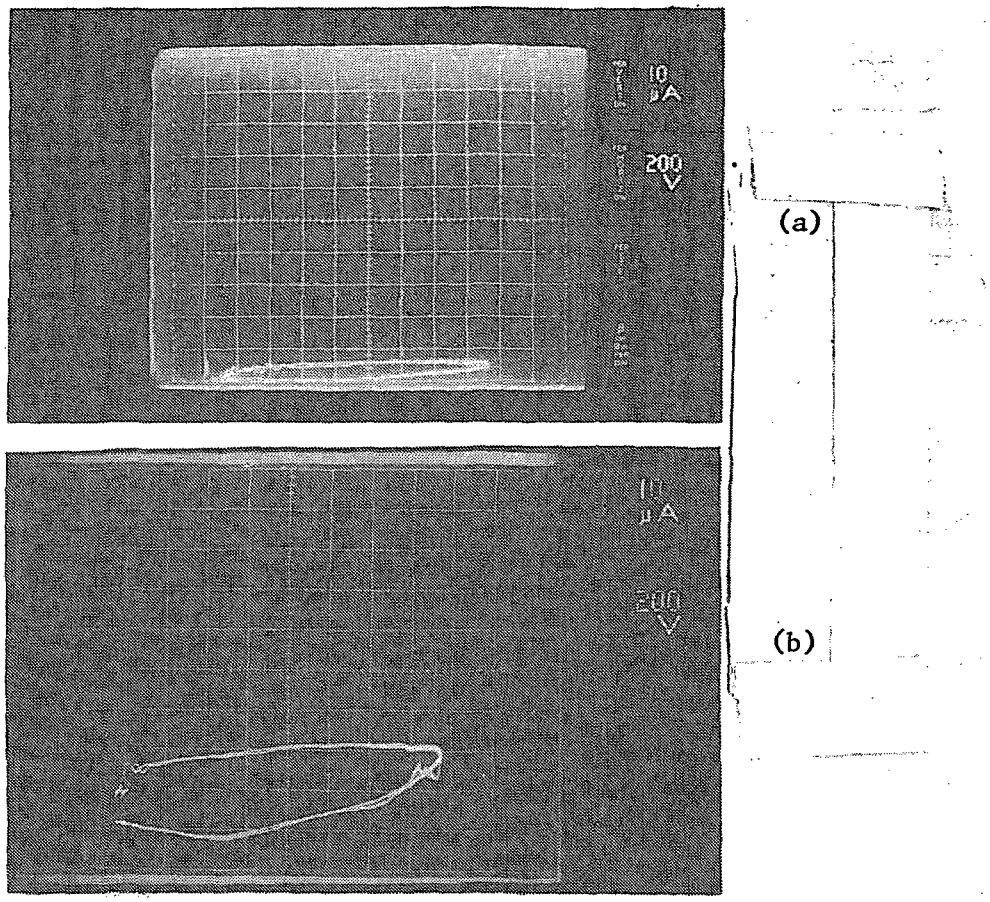


Figure 10. Two-point probe I-V characteristic of (a) B173 and (b) B233 in the dark. The wafers were grown with NH_3 in the gas stream.

TABLE 4. VAN DER PAUW MEASUREMENT

	300 K Mobility ($cm^2V^{-1}s^{-1}$)	77 K Mobility ($cm^2V^{-1}s^{-1}$)	(N_D-N_A) cm^{-3} From CV Data
B176	7238	64,540	$3x10^{15}$
B179	7151	43,690	$3x10^{15}$

layer punched through to the substrate. Van der Pauw measurements indicate a carrier concentration in the high 10^{13} cm^{-3} range with a 77 K mobility of 115,500 $cm^2V^{-1}s^{-1}$. Wafer B288, a 7.5-μm layer, had carrier concentration of 4-5x10^{14} cm^{-3} with 300 K and 77 K mobilities of 7786 $cm^2V^{-1}s^{-1}$ and 114,800 cm^2 $V^{-1}s^{-1}$, respectively. Of the 7.5 μm, 3 μm was 4-5x10^{14} cm^{-3} and 4.5 μm

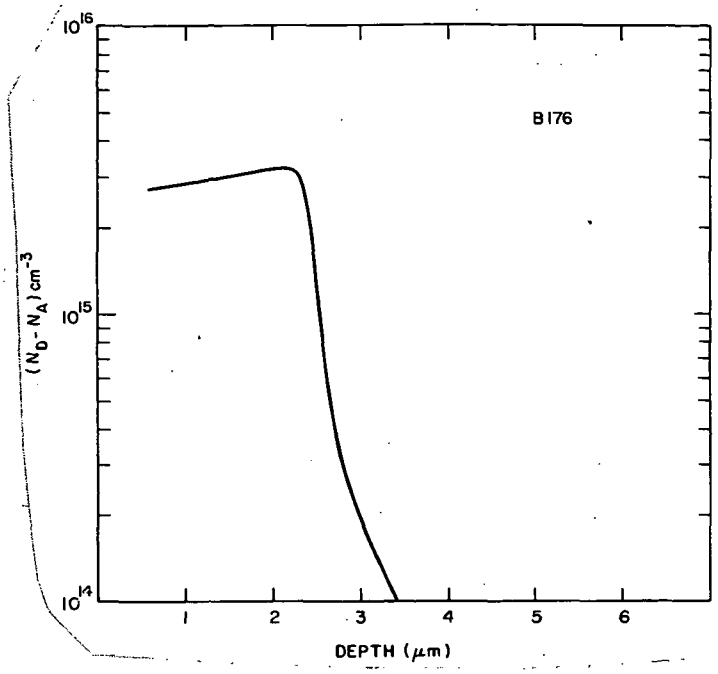


Figure 11. Carrier profile of undoped layer grown on buffer layer generated by adding NH_3 to gas stream. Buffer layer is 5.5 μm thick.

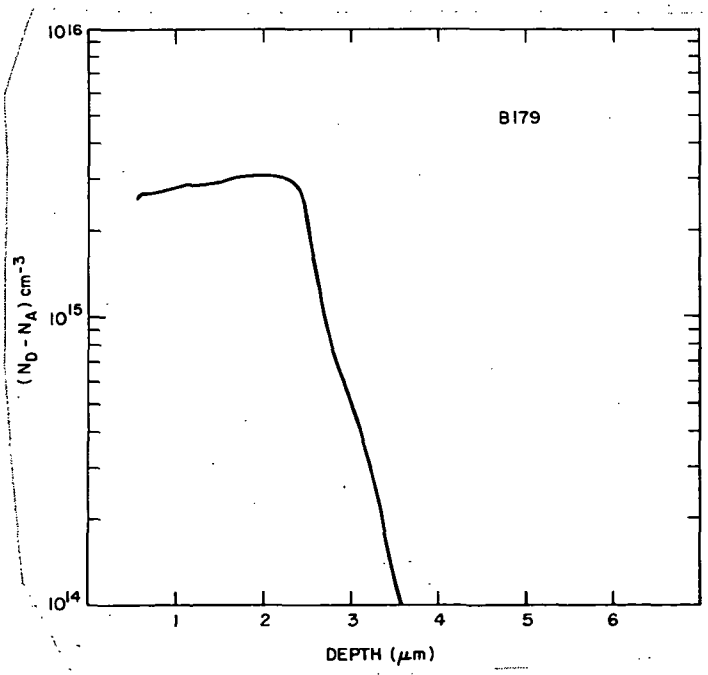


Figure 12. Carrier profile of 5.5-μm-thick undoped layer. Top 2.5 μm is $3x10^{15}$ cm^{-3} and bottom 3 μm is an "undoped" buffer layer.

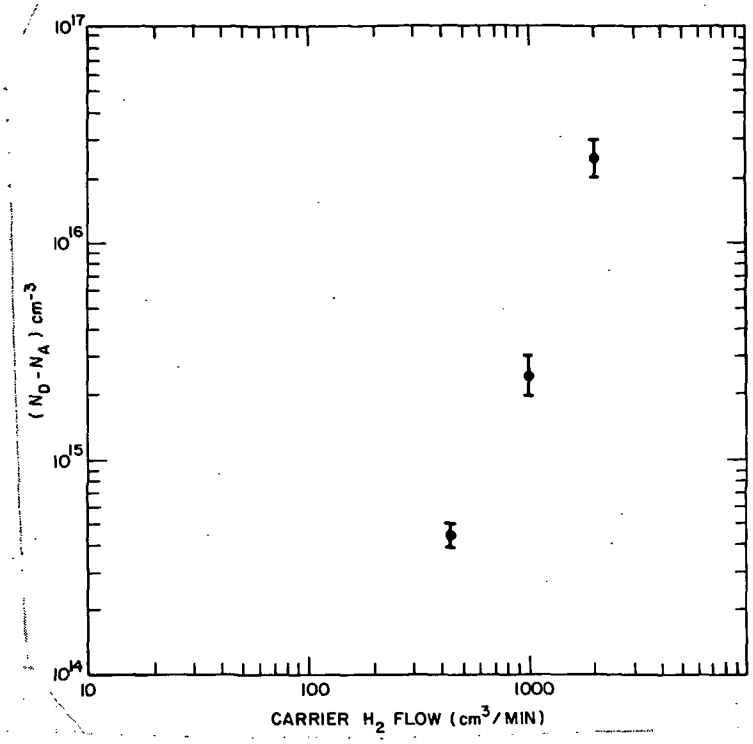


Figure 13. Effect of carrier flow rate on background effective donor concentration.

was an 'undoped' buffer. Figure 14 shows the doping profile. It is planned to introduce CrO_2Cl_2 to increase the resistivity of these layers. We are also investigating potential methods of Fe doping.

3. FET Wafers Grown by the Hydride Systems

The major materials effort was to grow a very large number of GaAs FET wafers. Most of the wafers did not have buffer layers. SI GaAs substrates from many vendors including Laser Diode*, Morgan**, and Sumitomo† were used. Thermal conversion under our growth ambient (715°C and AsH_3 overpressure) was observed on several substrate lots which were subsequently rejected. No major differences in substrate quality from different vendors were apparent. Devices from several wafers were superior to the majority, but it could not be ascertained whether this was due to the substrate or epitaxy.

*Laser Diode Laboratories, Metuchen, NJ.
**Morgan Semiconductor, Inc., Garland, TX.
†Sumitomo Electric Industries, Inc., Osaka, Japan.

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TABLE 5. HALL MEASUREMENT DATA ON SEVERAL GaAs TEST WAFERS

Wafer No.	$(N_D-N_A)cm^{-3}$ 300 K	$\mu-cm^2v^{-1}s^{-1}$ 300 K	$(N_D-N_A)cm^{-3}$ 77 K	$\mu-cm^2v^{-1}s^{-1}$ 77 K	Compensation Factor $(N_D+N_A)/(N_D-N_A)$	Comments
C261	$3.5x10^{15}$	7300	$3.3x10^{15}$	36,300	< 2	Background on undoped layer. No buffer.
C311	$3x10^{15}$	7400	$2.8x10^{15}$	34,500	~ 2	Background on undoped layer. No buffer.
C331	$1.6x10^{15}$	7800	$1.5x10^{15}$	43,500	< 2	Background on undoped layer. No buffer.
D91	$2.5x10^{16}$	5900	$2.3x10^{16}$	11,500	> 1	S-doped layer on undoped buffer.
D116	$7.7x10^{16}$	4600	$7x10^{16}$	5,500	~ 1.5	S-doped layer on undoped buffer.

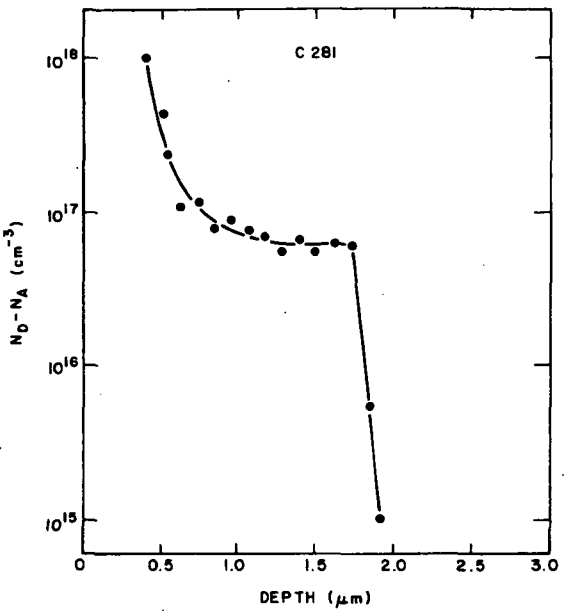


Figure 15. Carrier concentration profile of wafer C-281.

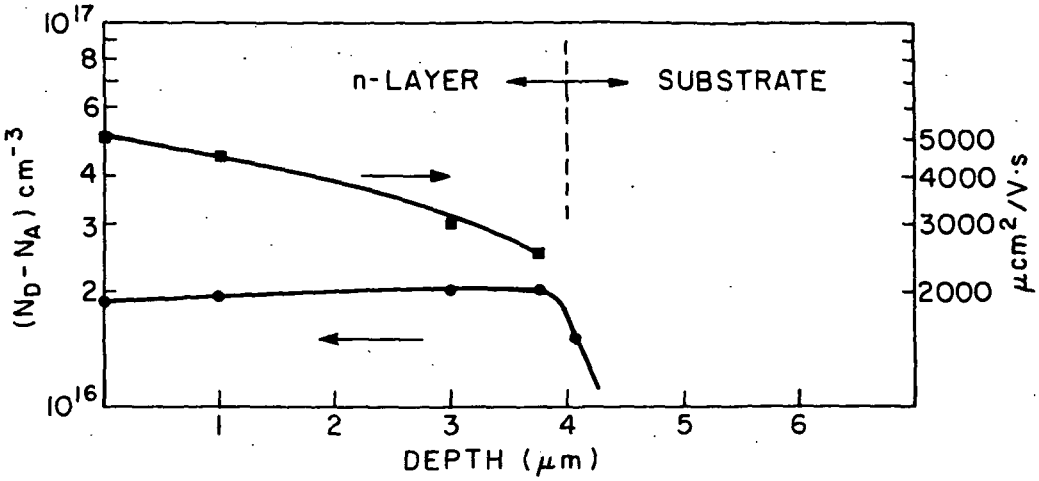
4. Trichloride Process

As described earlier, undoped (more correctly, not intentionally doped) buffer layers can be grown by $AsCl_3$ mole fraction control using the trichloride system. Figure 17 is an FET wafer with an undoped buffer layer. The doping level of the buffer layer was estimated to be about 4.5×10^{12} cm^{-3}.

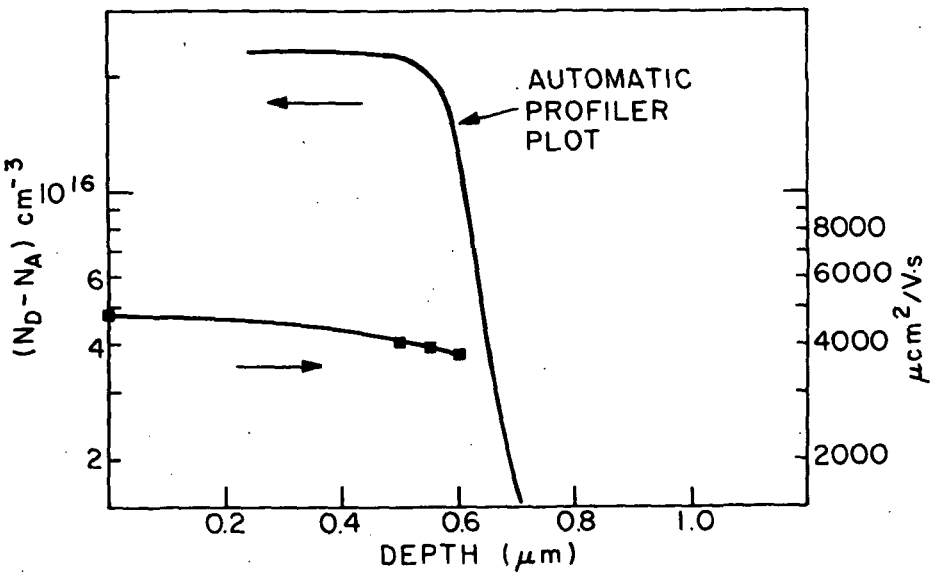
The resistivity of the undoped buffer layer was estimated by making transport measurements of the high-resistivity substrate before and after layer growth. Figure 18 is a plot of $\rho T^{1.5}$ as a function of 1000/T' for a Nikkei-Kako (NK) Cr-doped substrate from dark conductivity measurements. T' is a modified temperature given by:

$$T' = T \frac{E_g(300\ K)}{E_g(T)}$$

where $E_g(T)$ is the energy gap at a temperature of T (Kelvin). This assumes that relative energies of the impurity levels are proportional to the energy gap. Instead of correcting energies for thermal variations, the correction is made on kT since the energy differences are always divided by kT in expressions for resistivity. A straight line fit to these data indicates an activation energy on the order of 0.74 eV which is close to the O-level in GaAs (0.72 eV).



(a)



(b)

Figure 16. (a) Mobility and carrier profile measured by stripe-measure process, (b) mobility profile using Schottky-gated van der Pauw.

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Figure 19 shows the $\rho T^{1.5}$ - 1000/T' characteristics of the NK substrate repeated from the previous figure. The points, however, represent the data obtained from a dark conductivity measurement carried out on an undoped epitaxial SI layer (D80) grown on an NK substrate. This undoped layer was grown using the $AsCl_3/Ga/H_2$ process. The layer thickness was 6 μm and the substrate thickness 318 μm. Note that the data points for the composite structure fit reasonably well to the substrate characteristic. For these layer thicknesses, we can compute that ρ (buffer) $\geq$ 0.2 ρ (substrate) if we assume that the effect of the total layer resistance has to be about 10 times the substrate resistance to be unobservable. This puts a lower bound of 5×10^5 Ω-cm for the buffer layer resistance, which is adequate for device applications.

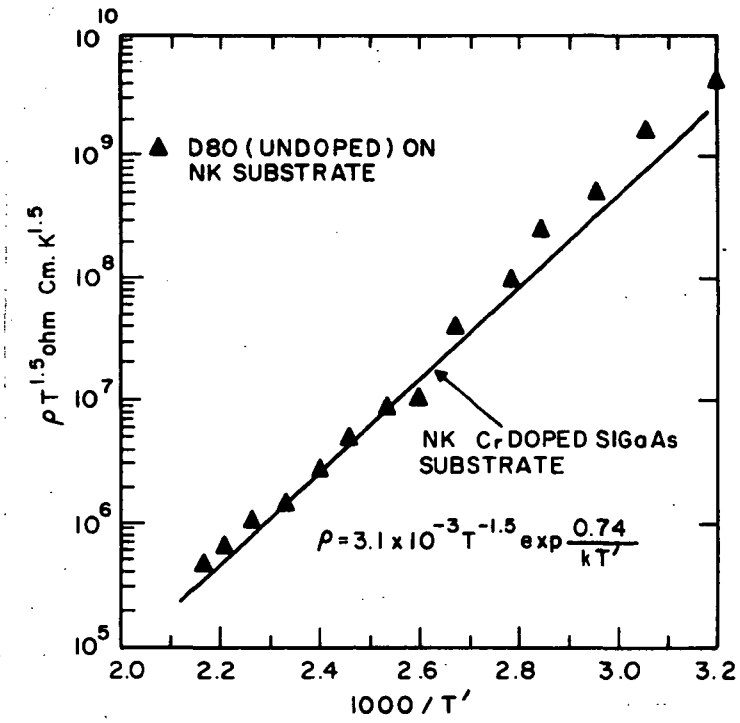

Figure 19. $\rho T^{1.5}$ data points for D80 on NK substrate. The straight line is the characteristic of the substrate alone.

SECTION III

MATERIALS RESEARCH ON ION IMPLANTATION

A. INTRODUCTION

One of the major reasons for the development of a technology for the epitaxial growth of SI GaAs is to use this layer as starting material for ion implantation. If high-quality, high-resistivity epitaxial layers can be repeatably grown on a variety of commercial bulk-grown SI substrates, more reproducible results can be obtained by ion implantation. We are currently investigating implantation of ^{28}Si over an energy range of 50 keV to 1.6 MeV into both commercial semi-insulating GaAs and into epitaxial buffer layers grown thereon. This implantation effort is supported in part with RCA funds and by an Office of Naval Research supported effort (N00014-78-C-0367). This section is included in this report because of its relevance to future Ku-band FET efforts.

B. 50- TO 250-keV IMPLANTATION

Implantation in this energy range was carried out using the machine at RCA Laboratories. The results obtained to date are described below.

1. Post-Implant Anneal

The post-implant annealing of GaAs to remove implantation damage and activate the implanted species is generally difficult since GaAs tends to dissociate at the commonly used anneal temperatures of 800 to 900°C. Dielectric encapsulation (SiO_2, Si_3N_4, AlN, etc.) has been used to prevent dissociation, but this often results in poor wafer surface due to outdiffusion of Ga or As into the encapsulant or uncontrolled indiffusion into GaAs. This is particularly detrimental to the high-quality layers required for GaAs FETs and planar Schottky varactors. We have developed a method for annealing implanted wafers without encapsulation under arsenic overpressure. This procedure has been very successful, and implanted wafers with excellent surface morphology have been obtained.

2. Carrier Concentration, Mobility, and Activation Efficiency

Implanted samples were characterized by sheet resistance and Hall measurements. Table 6 shows results obtained on S implantation to generate n- and n^+-layers. The samples marked with a star describe implantation into epitaxial buffer layers (high resistivity) grown on SI GaAs substrates. In general, implantation into epitaxial-buffer layers leads to more consistency and superior mobility for a given carrier concentration. When the substrate is of good quality (sample 45E), results comparable to implantation into epitaxial buffers are obtained.

Figure 20 is a plot of the 300 K electron mobility of a number of implant runs. Theoretical curves for various compensation factors are also shown. Figure 21 is a plot of the average carrier concentration as a function of implant dose. Note the saturation at higher dose levels. All implants were annealed without encapsulation under arsenic overpressure at 825°C for 20 minutes. The surface morphology of annealed wafers was excellent.

Table 7 summarizes the implantation of ^{28}Si into GaAs, using the same format as in Table 6, and basically the same conclusions apply. The major difference between implantation of S and Si is that Si-implanted layers are more reproducible and follow LSS theory more closely. Figure 22 shows the carrier density-implant dose curve for Si implantation. The data point indicated by the unfilled circle was annealed at 1000°C. The remaining data points correspond to annealing at 825°C. The anneal time was 20 minutes in all cases.

3. Carrier-Concentration Profile

Figure 23 shows the carrier concentration density profile of a Si-implanted sample as measured on automatic C-V impurity profile equipment. The implantation dose and energy level are 3.5×10^{12} at./cm^2 and 200 keV, respectively. The distribution is nearly Gaussian with a peak occurring at a depth of 0.17 μm below the surface and a standard deviation of about 0.07 μm. Figure 24 shows the profile of a multiple Si-implanted sample obtained from C-V measurement. The doping density toward the surface was increased by the low-energy implantation to result in a nearly constant carrier concentration distribution.

TABLE 6. S IMPLANTATION IN GaAs

SAMPLE NUMBER	SUBSTRATE	ENERGY (keV)	DOSE (cm^{-2})	MOBILITY ($cm^2/V-s$)	APPOX. CARRIER CONC. (cm^{-3})	ACTIVATION EFF (%)
62B	SI (MM-G103)	200	4.0×10^{12}	3318	8.4×10^{16}	41.8
63B	Cr-n^-/SI* (A-141)	200	5.0×10^{12}	4053	1.8×10^{17}	72.4
10A	SI (LD)	200	5.0×10^{12}	3220	1.8×10^{17}	73.6
10D	(5-μm)n^-/SI*	200	5.0×10^{12}	4005	1.7×10^{17}	67.2
45A	(3-μm)n^-/SI* (C265)	250	7.0×10^{12}	4364	1.4×10^{17}	40.9
45E	SI (MX)	250	7.0×10^{12}	4067	1.5×10^{17}	46.9
45F	(10-μm)Cr-n^-/SI* (A90)	250	7.0×10^{12}	4331	1.2×10^{17}	37.1
19X	SI (LD)	200	7.0×10^{13}	3219	3.7×10^{17}	73.0
14C	SI (LD)	200	1.5×10^{13}	3230	2.5×10^{17}	32.8
64A	SI (MMG102)	200	2.0×10^{13}	2899	5.8×10^{17}	58.3
57	SI (XS3761)	200	1.0×10^{14}	3201	1.5×10^{18}	30.6
50A	SI (XS3761F)	200	5.0×10^{14}	2891	1.7×10^{18}	6.7

*Vapor-phase high-resistivity epitaxial layer grown on SI substrate.

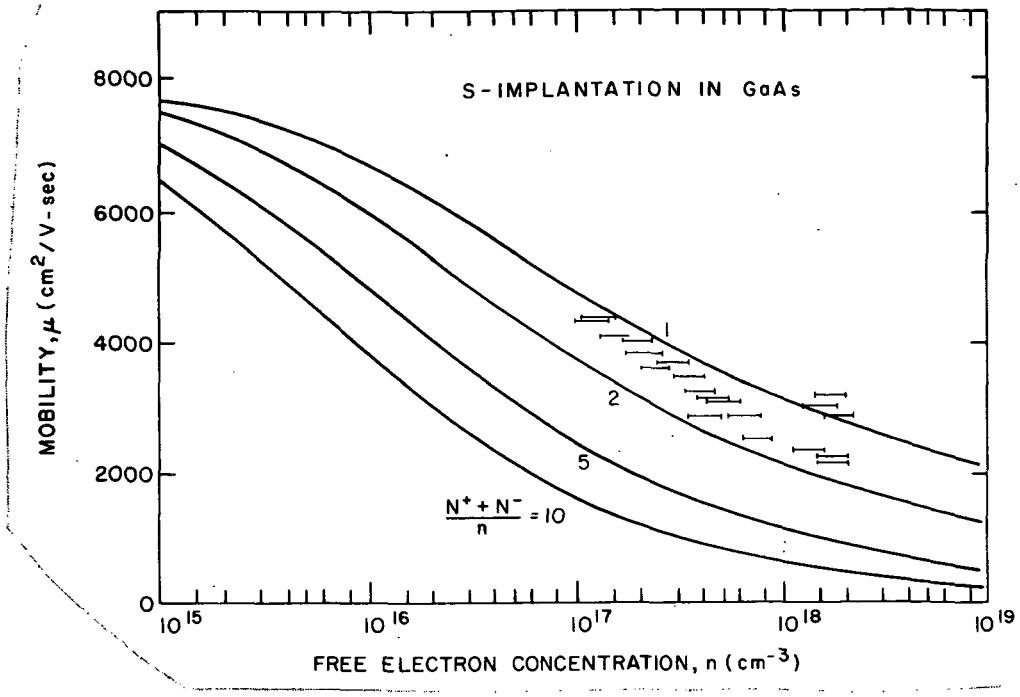

Figure 20. Mobility vs (N_D-N_A) for S implantation.

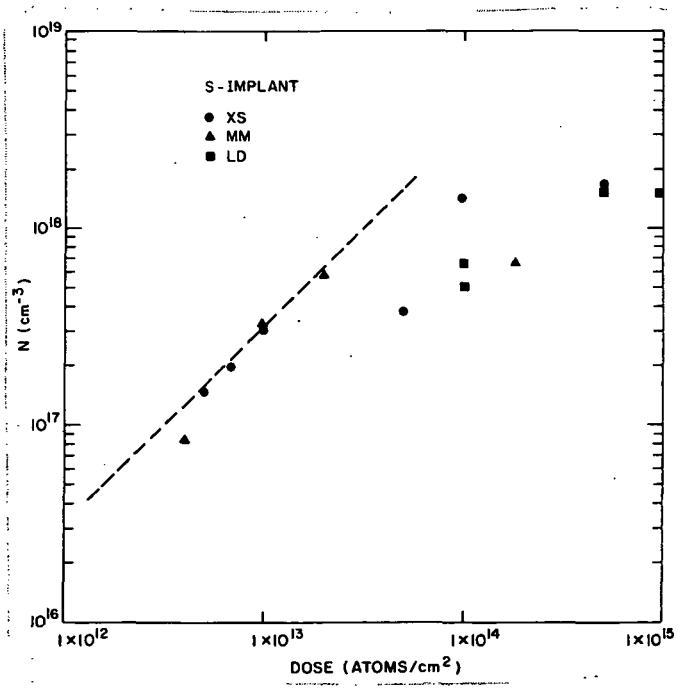

Figure 21. Carrier concentration vs dose characteristic for S implantation.

TABLE 7. Si IMPLANTATION IN GaAs

SAMPLE NUMBER	SUBSTRATE	ENERGY (keV)	DOSE (cm^{-2})	MOBILITY ($cm^2/V-s$)	APPROX. CARRIER CONC. (cm^{-3})	ACTIVATION EFF. (%)
A24A	6-μmn$^-$/SI* (D95)	200	3.0×10^{12}	4285	8.2×10^{16}	54.9
A35A	SI (XS3761)	200 70	3.0×10^{12} 1.5×10^{12}	3374	1.9×10^{17}	82.6
A35C	SI (XS3765F)	200 70	3.0×10^{12} 1.5×10^{12}	3630	1.7×10^{17}	76.8
A35D	5-μmn$^-$/SI* (D143)	200 70	3.0×10^{12} 1.5×10^{12}	4000	1.9×10^{17}	85.1
A28N	SI (XS3761F)	200	3.5×10^{12}	3740	1.6×10^{17}	90.3
A23A	Cr-n$^-$/SI* (A156)	200	4.0×10^{12}	3928	1.2×10^{17}	60.5
A3A	SI (MMG102)	200	4.0×10^{12}	3570	1.2×10^{17}	62.0
A26	SI (XS3765)	200 50	4.0×10^{12} 2.0×10^{12}	4000	1.5×10^{17}	60.5
A4B	SI (XS3761)	200	6.0×10^{12}	3222	1.9×10^{17}	64.7
A31	SI (XS3761)	200	2.0×10^{13}	2931	7.0×10^{17}	70.1
A6	SI (MMG102)	200	5.0×10^{13}	2049	1.1×10^{18}	37.0
A34	SI (XS3761F	200	1.0×10^{14}	2204	1.1×10^{18}	21.5
A44	SI (XS3761F)	70	1.0×10^{15}	1770	1.6×10^{18}	3.2

*Vapor-phase high-resistivity epitaxial layer grown on SI substrate.

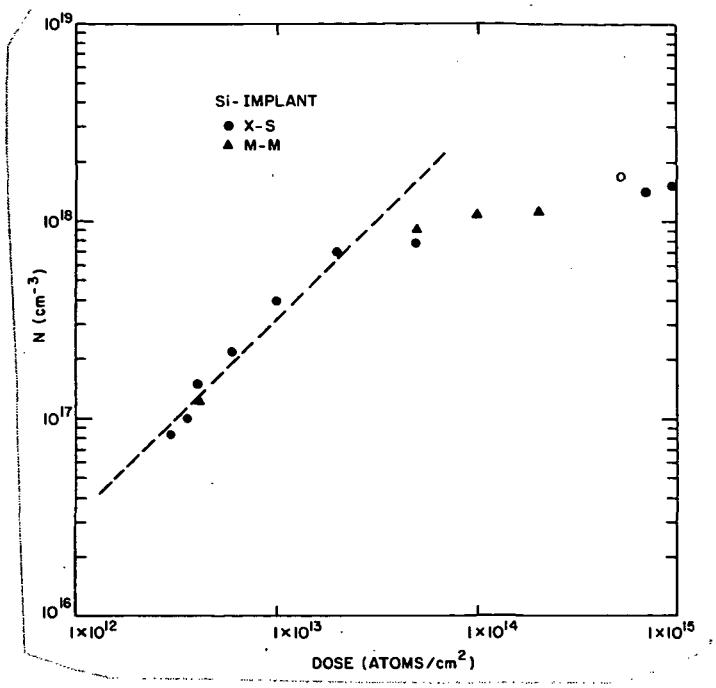

Figure 22. Carrier concentration vs dose characteristic for Si implantation.

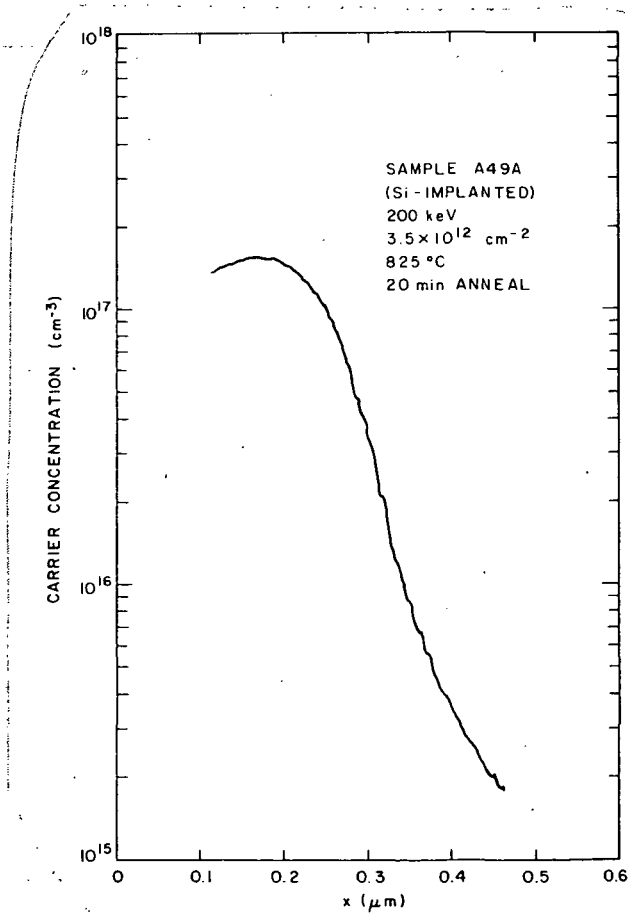

Figure 23. Carrier profile for single-energy Si implant.

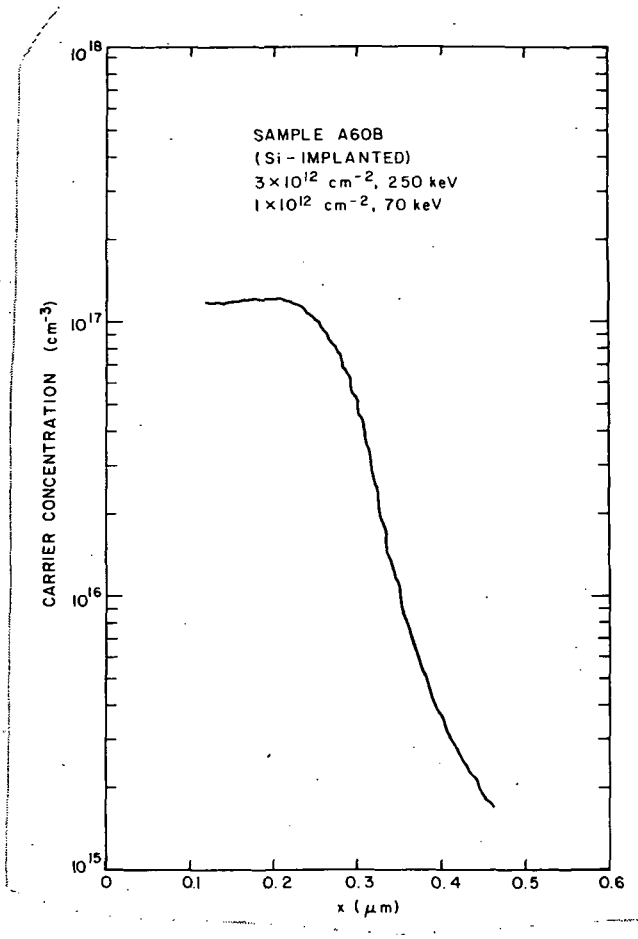

Figure 24. Carrier profile for dual Si implant.

4. Contact Resistivity Measurement

Contact resistivity of ohmic contacts made onto GaAs has been reported to be inversely proportional to the carrier density of GaAs. The contact resistivities of Au-Ge ohmic contacts on ion-implanted GaAs with different dose levels were studied by use of the TLM technique. Contact resistivity of 8×10^{-7} Ω-cm^2 was measured on heavily implanted samples, and $2\text{-}5\times10^{-5}$ Ω-cm^2 on lightly implanted samples. The carrier concentrations of the high- and low-dose samples were $1\text{-}2\times10^{18}$/cm^3 and $1\text{-}2\times10^{17}$/cm^3, respectively. The much lower contact resistivity of heavily implanted samples indicates that selective implantation can be applied in the device processing to minimize contact resistance. Results of measured contact resistivity and sheet resistance on a number of S- and Si-implanted GaAs samples are shown in Table 8.

TABLE 8. SHEET RESISTIVITY AND SPECIFIC CONTACT RESISTANCE

SAMPLE	IMPLANTED ION	DOSAGE (cm^{-2})	ENERGY (keV)	METAL CONTACT	SINTER CONDITION	ρ_s ($\Omega/\square$)	ρ_c (Ω-cm^{-2})
A28D	Si	3.5×10^{12}	200	1500 Å Au-Ge 500 Å Ni	450°C, 1 min Forming Gas	514	3.9×10^{-5}
A35B	Si	3.0×10^{12} 1.5×10^{12}	200 70	1500 Å Au-Ge 500 Å Ni	450°C, 1 min Forming Gas	589	1.2×10^{-5}
A29	Si	5.0×10^{14} 2.0×10^{14}	200 70	1500 Å Au-Ge 500 Å Ni	450°C, 1 min Forming Gas	114	7.8×10^{-7}
5A	S	3.0×10^{13}	200	1500 Å Au-Ge 500 Å Ni	450°C, 1 min Forming Gas	259	2.4×10^{-5}
10D	S	5.0×10^{12}	200	60 Å Ni 1500 Å Au-Ge 600 Å Ni-Au	450°C, 1 min Forming Gas	432	6.0×10^{-5}
47A	S	1×10^{15}	250	750 Å Au-Ge 250 Å Ni	450°C, 1 min Forming Gas	89	4.0×10^{-6}

C. HIGH-ENERGY IMPLANTATION

High-energy (>500 keV) implantation of $^{28}Si^{+}$ into semi-insulating GaAs substrates was performed using a 3-MeV (max) Van de Graaff implanter equipped with a cold cathode discharge ion source. This machine is located at the Fusion Energy Corporation, Princeton, NJ. Three batches of samples were implanted. Initial results being analyzed are very encouraging.

1. Implantation Conditions

The first batch of samples was high-dose ($\sim 3 \times 10^{15}$ at./cm^2) implanted at energy levels from 600 keV to 1.2 MeV; the second batch was implanted at 1 MeV with doses varying from 1.5×10^{13} to 5.0×10^{15} at./cm^2; and the third batch was of multiple implantations at several energy levels in an attempt to obtain a 1-μm flat profile. The implant conditions were worked out for forming 1-μm-deep Si-doped layers in GaAs with nearly constant doping throughout the layer.

Five implants ranging from 40 to 900 keV are used to construct this layer. A calculated plot of the expected doping profile is shown in Fig. 25 using a linear ordinate scale and in Fig. 26 using a log ordinate scale. Figure 27 shows plots of R_p and ΔR_p obtained either experimentally from SIMS measurements on implanted wafers or calculated using the Gibbons and Johnson implementation of the LSS theory and the electron stopping power data of Northcliffe and Schilling. At this time, the calculated R_p and ΔR_p values do not agree very well with experimental data. We therefore used extrapolated experimental curves for the determination of implant parameters to obtain a flat profile. Table 9 summarizes the implant conditions.

2. Evaluation of Implanted Wafers

The implanted GaAs wafers are being analyzed by SIMS, van der Pauw measurements, and differential C-V measurement. Figure 28 shows the SIMS profiles of the high-dose, single implantation. The profiles clearly show the depth dependence of Si atoms introduced into GaAs on the energies used. The projected ranges are, however, higher than those computed as indicated in Fig. 27. Following thermal annealing at 825°C for 20 min, sheet resistance and Hall measurements of the high-dose (3×10^{15} at./cm^2) implanted samples show that the mobilities vary between 1500 and 2200 cm^2/V-s and the sheet resistances lie between 44 and 110 Ω/□. After thermal annealing at 970°C for 20 min, sheet resistances

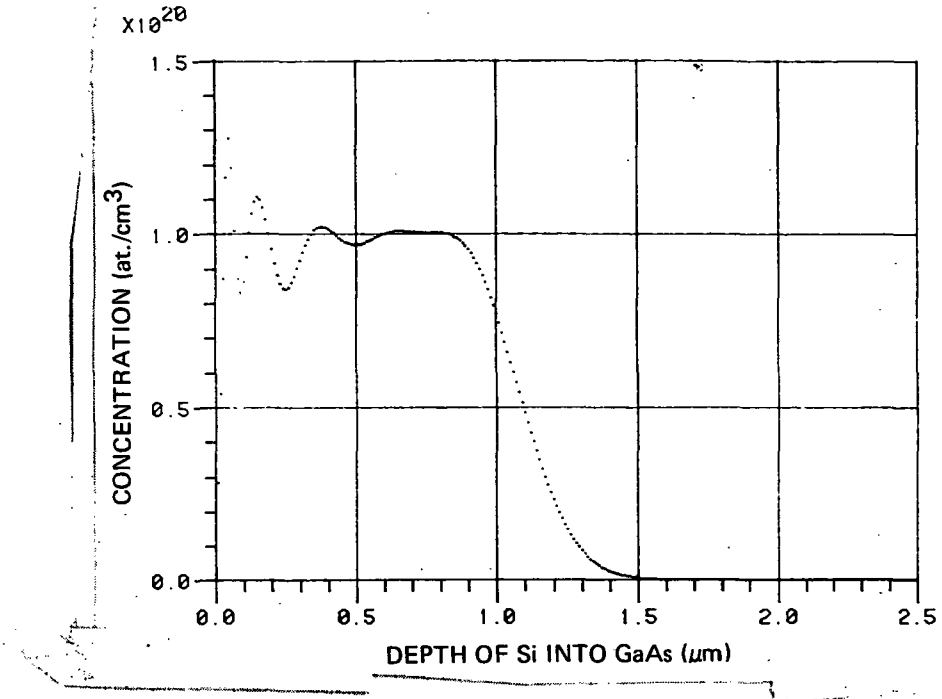

Figure 25. Computed multi-implant doping profile - linear ordinate scale.

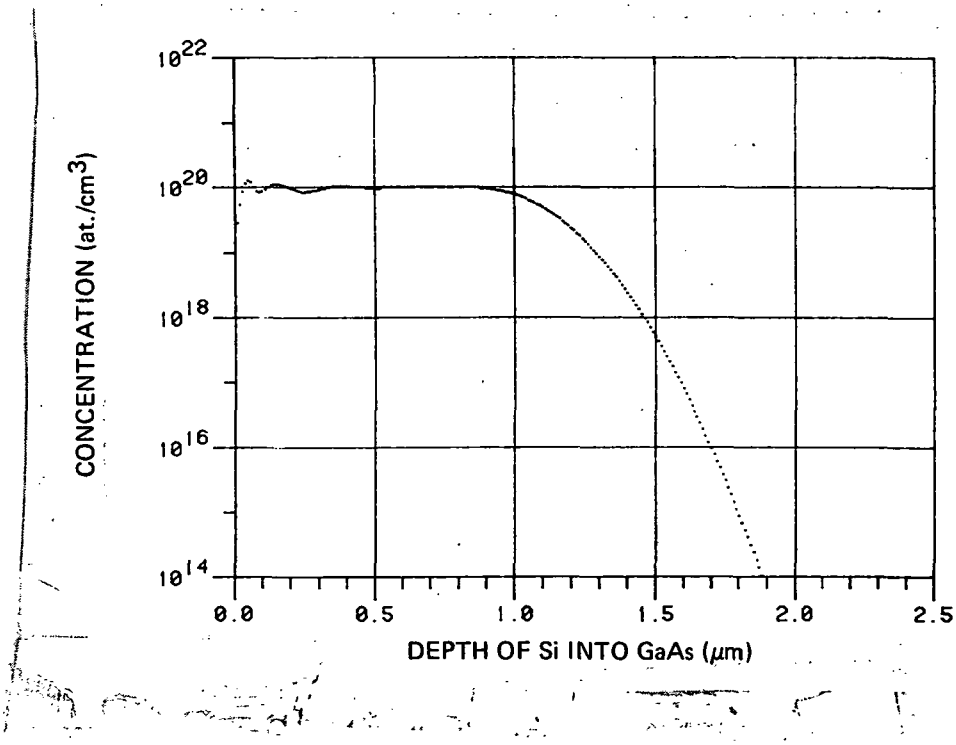

Figure 26. Computed multi-implant doping profile - log ordinate scale.

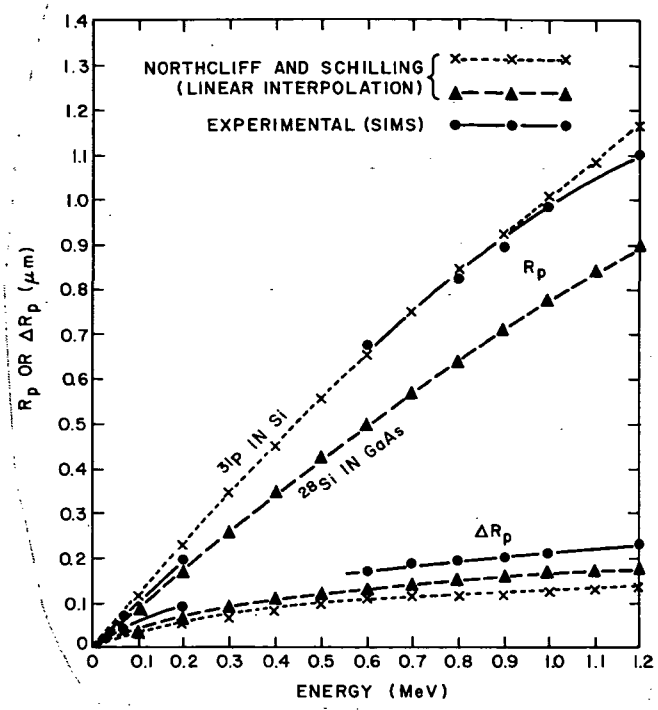

Figure 27. R_p and ΔR_p for ^{28}Si in GaAs. (Experimental values measured from SIMS profiles of actual implants. ΔR_p = full width at 0.607 x N_{max}).

TABLE 9. IMPLANT CONDITIONS FOR FLAT PROFILE OF Si IN GaAs

Parameters	Energy (keV)				
	40	120	280	500	900
R_p (μm)	0.0466	0.1375	0.3195	0.5500	0.8860
ΔR_p (μm)	0.0199	0.0600	0.1050	0.1500	0.1900
N_{max} (cm^{-2})	9.47×10^{19}	9.08×10^{19}	7.23×10^{19}	7.26×10^{19}	9.09×10^{19}
N_{dose} (cm^{-2})	4.70×10^{14}	1.35×10^{15}	1.9×10^{15}	2.73×10^{15}	4.33×10^{15}
Dose No.	303.6	872.0	1227	550.2	872.6
Scale	6E-6	6E-6	6E-6	6E-6	6E-6

Area = 24.19 cm^2 (Labs machine)

Area = 7.56 cm^2 (FEC machine)

Total Dose = $1.08 \times 10^{16}/cm^2$

Conc. Level = $1.00 \times 10^{20}/cm^3$

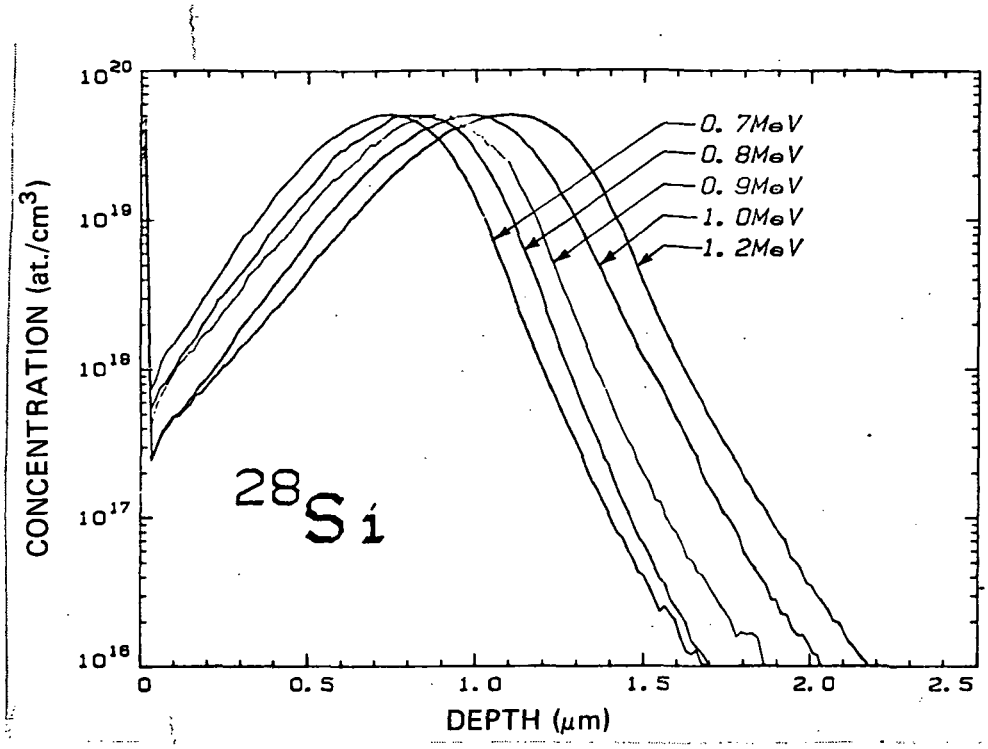

Figure 28. SIMS profile of high-dose single implants.

of 27 and 22 Ω/□ with corresponding mobilities of 1500 and 1320 cm^2/V-s were measured. These results are comparable or better than those achieved with low-energy implantation. The samples were encapsulated with 2000-Å-thick sputtered Si_3N_4 during thermal annealing in a N_2 atmosphere. Figure 29 summarizes these results on high-energy single implants being evaluated to date.

A differential C-V technique was used in evaluation of electron density profiles of low-dose, high-energy implanted samples. This technique consists of a combination of C-V measurements and controlled layer removal by chemical etching. Figure 30 shows the depth distribution of carrier concentration measured using this technique. The circular points are normalized data from SIMS measurement on a high-dose, single-implanted (600 keV) unannealed sample. The double-hump behavior is a result of lack of an implantation in the middle (300 to 500 keV) energy region. Sheet carrier concentration and Hall measurements on the sample show that the overall mobility was 3633 cm^2/V-s, the sheet carrier concentration was 9.2×10^{12} at./cm^2, and the activation efficiency was 27.5%. Experiments are being continued on annealing and analyzing the remaining single and multiple high-energy implanted samples.

Figure 31 shows the SIMS profile of high-dose multiple implanted wafers. Table 10 shows the implantation parameters for H-24, H-25, and H-28. These

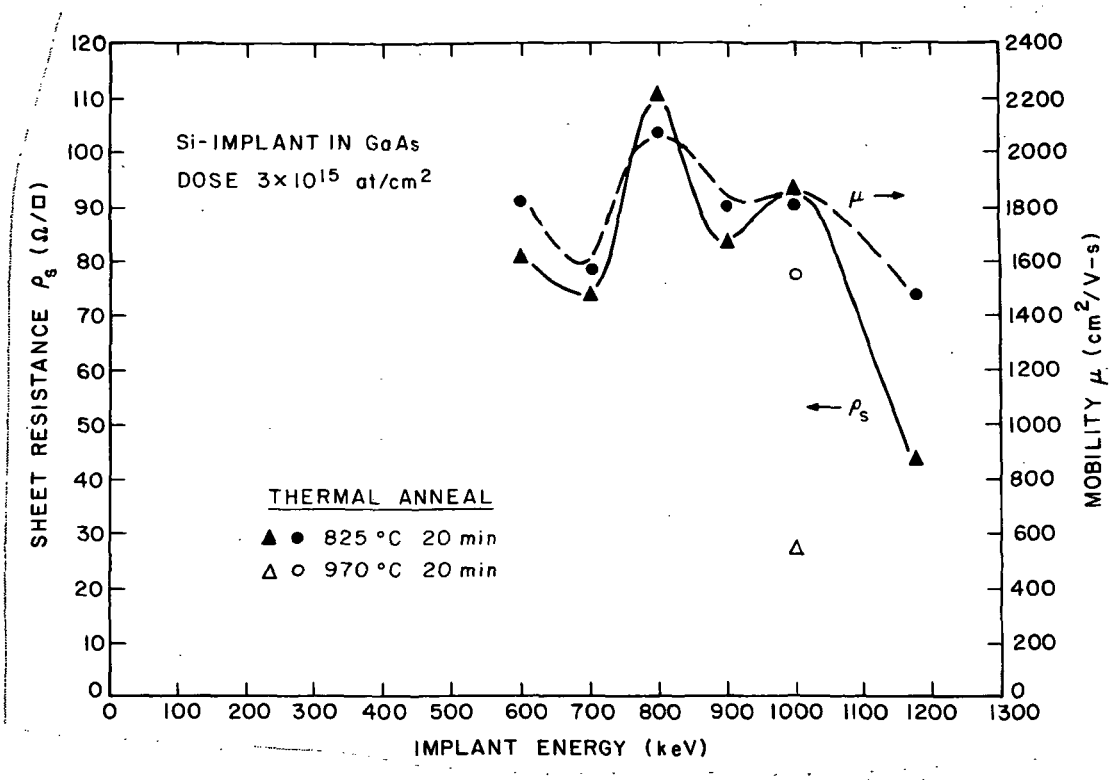

Figure 29. Mobility and sheet resistance measured after thermal annealing for samples implanted at high energy levels.

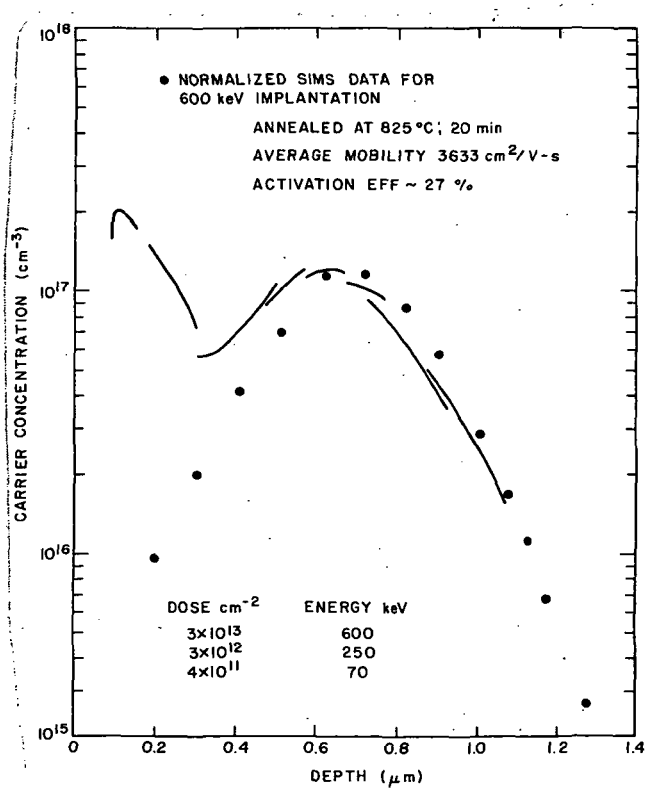

Figure 30. Composite doping profile and normalized SIMS data for multiple implantation.

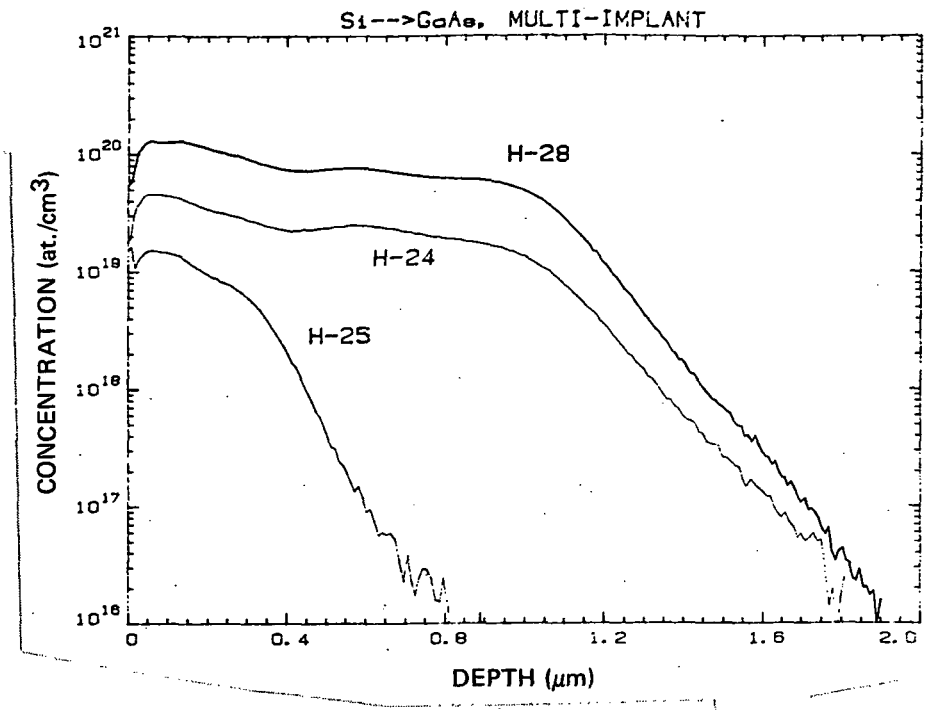

Figure 31. SIMS profile for multiple implants. See Table 10 for implant conditions.

TABLE 10. MULTIPLE IMPLANT PARAMETERS

H-24		H-25		H-28	
Energy (keV)	Dose (cm^{-2})	Energy (keV)	Dose (cm^{-2})	Energy (keV)	Dose (cm^{-2})
40	$1.4x10^{14}$	40	$4.7x10^{13}$	40	$4.7x10^{14}$
120	$4x10^{14}$	120	$1.35x10^{13}$	120	$1.35x10^{15}$
280	$5.7x10^{14}$	280	$1.9x10^{14}$	280	$1.9x10^{15}$
500	$8.2x10^{14}$	500	$2.7x10^{14}$	500	$2.7x10^{15}$
900	$1.3x10^{15}$	900	$4.3x10^{14}$	900	$4.3x10^{15}$

profiles were obtained before annealing. Note that profiles of H-24 and H-28 are in reasonable agreement with the shape of the calculated profile in Fig. 25. H-25 is much thinner than expected, and further studies are being carried out.

Figure 32 shows the SIMS profile for 1-MeV implantation at three doses. This will be used to calibrate and obtain dose-peak concentration data.

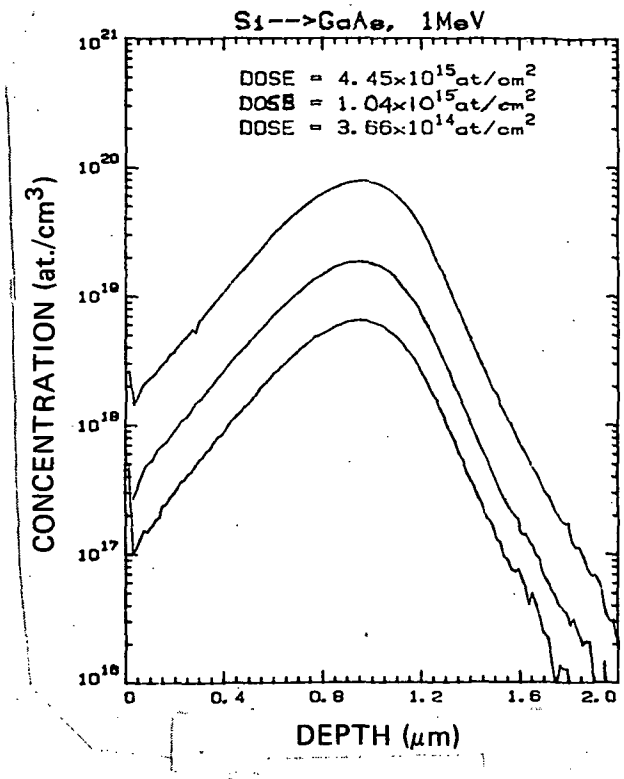

Figure 32. SIMS profile for 1-MeV implantation at three dose levels.

SECTION IV

DEVICE RESEARCH

A. BASIC LARGE-SIGNAL MODEL

A previously developed large-signal model is described in this section to provide background for discussion. Figure 33 is a schematic diagram of the depletion region boundary under the gate for different gate voltages. With a small forward bias on the gate, the depletion region profile is similar to boundary 1 in Fig. 33. The velocity is saturated at the drain end of the gate where the depletion depth is $(T - X_o)$. As the gate is reverse-biased and the reverse bias increases, the depletion boundary moves downward from profile 1 to profile 2 and so on until the channel pinches off. The dc bias on the gate puts the depletion layer boundary in the vicinity of profile 3. The rf swing moves the depletion boundary from profile 1 to pinch-off. Very little input power is dissipated in the channel in moving the boundary from 1 to 2. When the gate is biased by a superposition of dc and rf voltage, the depletion boundary moves sinusoidally with respect to profile 3. Hence, the charge under the gate also varies sinusoidally as:

$$Q = \frac{1}{2} Q_o \ (1-\sin\omega t) \tag{1}$$

where $Q_o = neWX_o\ell_g$, n is free carrier density, W is channel width, ℓ_g is gate length, and X_o is active channel thickness. The input circuit current is

$$I_{in} = \frac{dQ}{dt} = -\ 1/2\ Q_o\omega \cos \omega t \tag{2}$$

The resistance of the channel through which the input current flows varies from a relatively low value in the forward bias portion of the cycle to a value approaching infinity at pinch-off. We can evaluate this resistance by noting that the channel is an RC transmission line with the drain end open-circuited. The input impedance Z_t of an open-ended RC transmission line is given by

$$Z_t = Z_o/\text{Tanh}\ \left(\sqrt{j\omega R'C'L}\right) \tag{3}$$

where $Z_o = \sqrt{\frac{R'}{j\omega C'}}$

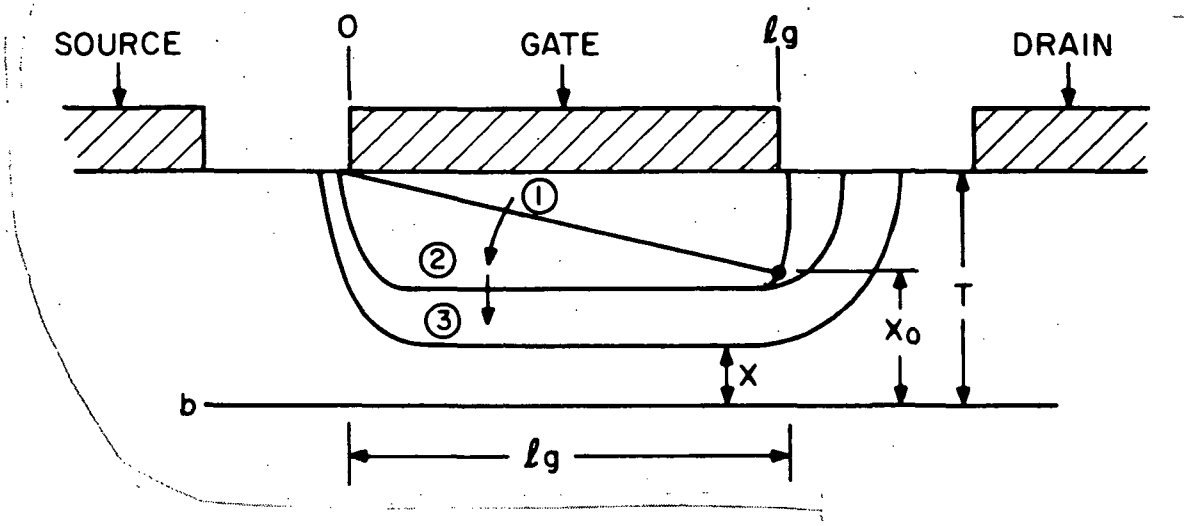

Figure 33. Cross section of gate with various states of carrier depletion of the channel.

R' and C' are the resistance and capacitance per unit length along the line, respectively. For typical FETs, $X_o T/\ell_2^2 > 0.01$ and the argument of the Tanh function is less than unity. Thus, we can approximate

$$Z_t = \frac{1}{3} R + \frac{1}{j\omega C} \tag{4}$$

where R and C are total channel resistance and total gate-channel capacitance, respectively. The effective channel series resistance is thus 1/3 the total channel resistance under the gate

$$R_{eff}(t) = 1/3\ R_{channel}(t) = 1/3\ \frac{\ell_g^2}{\mu Q_o} = \frac{2}{3}\left[\frac{\ell_g^2}{\mu Q_o}\right]\frac{1}{(1-\sin \omega t)} \tag{5}$$

where μ is the electron drift mobility.

The average input power is given by

$$P_{in} = 1/T \int_{-T/2}^{T/2} I_{in}^2 R_{eff}(t)dt = \frac{1}{6}\frac{w^2}{\mu}\ell_g^2 Q_o \tag{6}$$

The spreading resistance from the source end of the channel increases the effective series resistance. We will account for this by using a multiplying factor Σ for Eq. (6)

$$\Sigma = (1 + \ell_s/\ell_g) \tag{7}$$

where ℓ_s is the source-gate separation.

The dc and rf I-V characteristics are as shown in Fig. 34. The rf output current is given by

$$I_{out} = -\frac{1}{2}\frac{Q_o v_m}{\ell_g}\cos \omega t \tag{8}$$

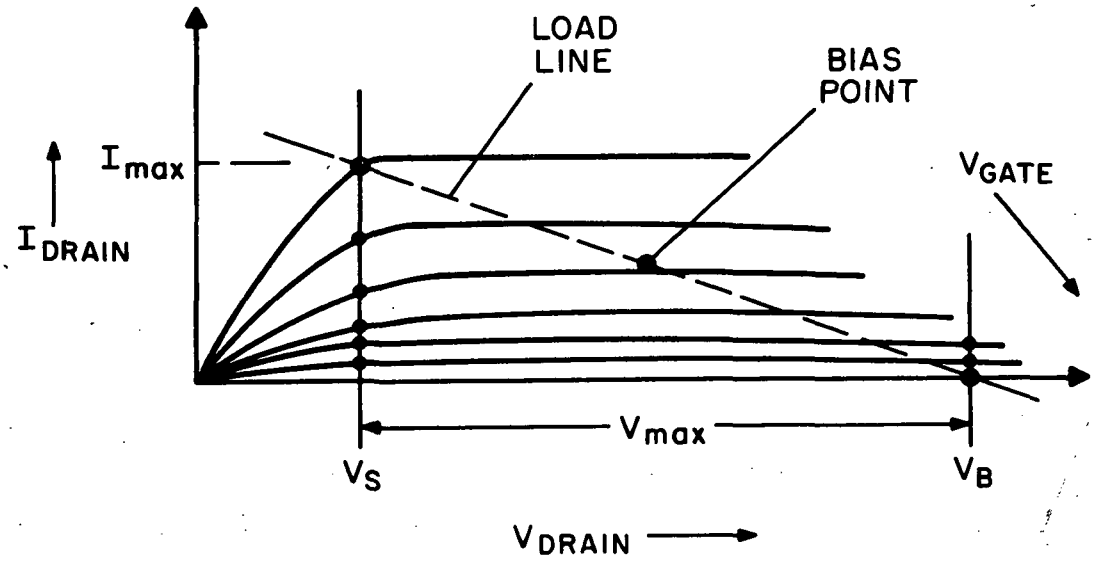

Figure 34. I-V characteristic and load line of FET.

The rf output voltage is given by

$$V_{out} = \frac{1}{2} V_{max} \cos \omega t \tag{9}$$

where v_m is maximum drift velocity, $V_{max} = (V_B - V_P - V_s)\rho$, V_B is breakdown voltage V_P is pinch-off voltage, V_s is saturation voltage, and ρ is a phase shift degradation factor. The average output power is obtained from

$$P_{out} = \frac{-1}{T}\int_{-T/2}^{T/2} I_{out} V_{out} dt = \frac{1}{8} V_{max} Q_o v_m/\ell_g \tag{10}$$

A finite output conductance G_o absorbs some of the power supplied by the device. Treating G_o as a lossy shunt element across the load, the output power is reduced by a factor Γ:

$$\Gamma = 1 - \frac{G_o \ell_g}{Q_o v_m} V_{max} \tag{11}$$

For X-band GaAs FETs, Γ is on the order of 0.8.

The output power of the GaAs FET can be calculated from Eqs. (10) and (11). Notice that Q_o can be approximated by

$$Q_o = ne\ w\ T\ \ell_g \tag{12}$$

Therefore,

$$P_{out} = \frac{1}{8} V_{max}\ ne\ w\ T\ V_m\ \Gamma \tag{13}$$

The power gain is obtained from dividing the output power by the input power.

$$P_{out}/P_{in} = \frac{3}{4} \left[\frac{\mu v_m}{\omega^2 \ell_g^3}\right] V_{max}\ \frac{\Gamma}{\Sigma} \tag{14}$$

$\Gamma \leq 1$ and $\Sigma > 1$.

The maximum power gain increases with low-field mobility μ, maximum drift velocity v_m, breakdown voltage V_B, and is proportional to ℓ_g^{-3}. Γ and Σ can be calculated from Eqs. (11) and (7), respectively,

$$\Gamma = 0.81$$

and

$$\Sigma = 1 + \frac{0.3 \times 10^{-4}}{\ell_g}$$

There, the power gain can be expressed as

$$\text{Power gain} = \frac{5.07 \times 10^3}{f^2 \ell_g^3 \left(1 + \frac{0.3}{\ell_g}\right)} \tag{15}$$

where f is in GHz, ℓ_g is in μm.

Equation (15) is plotted in Fig. 35. The expected device gain is plotted as a function of frequency for various gate lengths. For a fixed gate length the gain drops off at 6 dB per octave increase of frequency, as expected. The measured G_{max} of RCA's 2.5-μm gate length GaAs power FETs is also shown. The theoretical calculations agree fairly well with our experimental results.

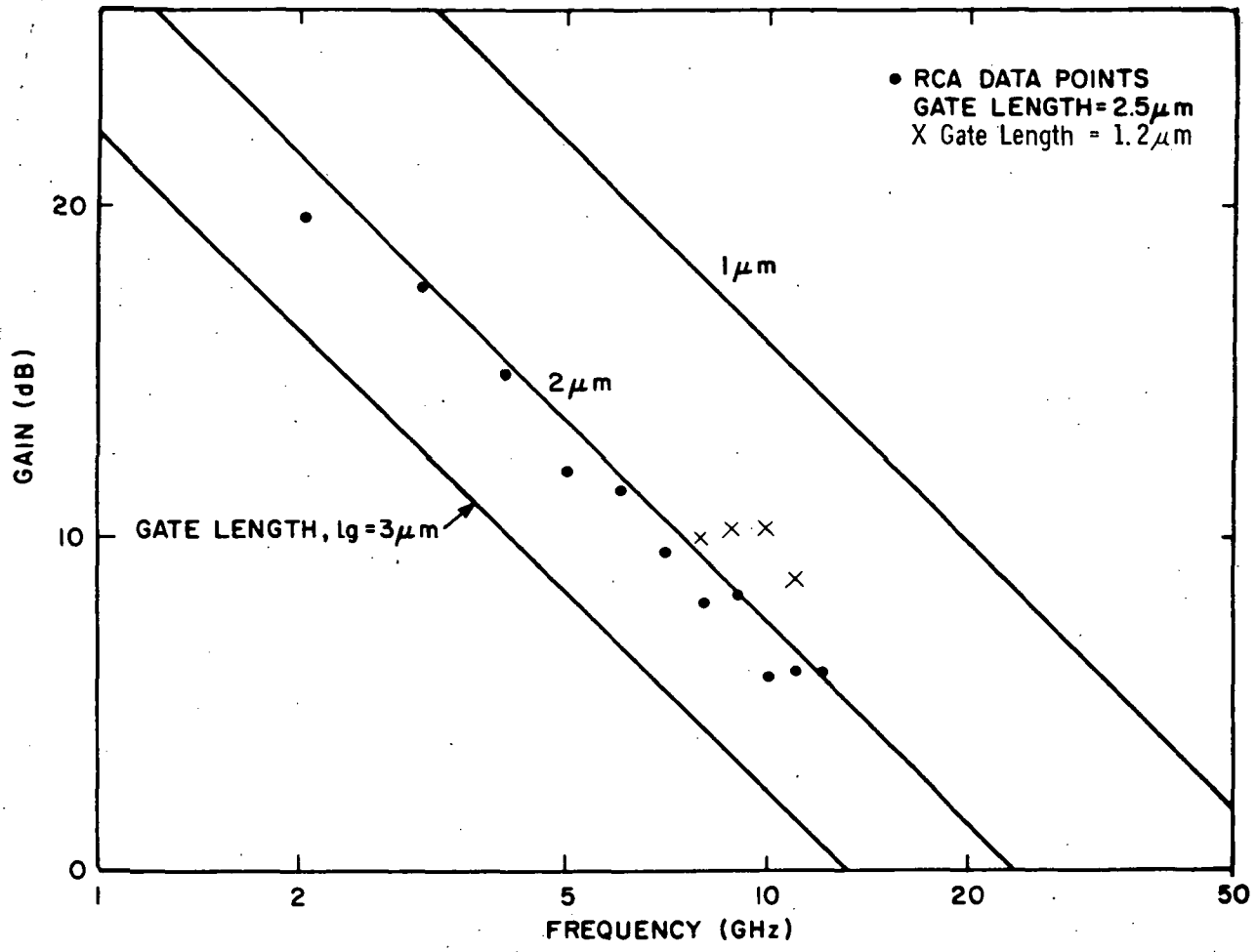

Figure 35. Small-signal gain versus frequency with gate length as parameter.

Notice that the above calculation did not include the degradation factors such as gate width limitation, ohmic contact resistance, parasitic capacitance effects, and parasitic source inductance effects. These factors will be discussed in a later section. When these factors are taken into account, we find that devices with 150-μm gate width and 1-μm gate length will provide a useful gain of approximately 10 dB at 10 GHz.

B. DEVICE DESIGN

The basic large-signal model can be used to derive a set of design rules. These rules serve as a guideline for the choice of carrier concentration, layer thickness, gate length, and gate width. In order to keep these rules simple and to retain a proper physical insight, we will employ some approximations based on experimental results. The results of these design guidelines have been confirmed experimentally both at RCA and at other laboratories.

Given a set of performance requirements such as output power, gain, and operating frequency, the required gate length can be derived from Eq. (15). Since Eq. (15) did not take into account the degradation factors such as ohmic contact resistance, parasitic impedances, and material nonuniformity, we will assume that an intrinsic gain of 20 dB is required. We will further assume that the gate length is larger than 0.3 μm. Thus, we will neglect the $0.3/\ell_g$ term in Eq. (15). This assumption will introduce less than a 3-dB error in gain. The frequency range in which this model is valid is about 2 to 20 GHz. With the above assumption, Eq. (15) now becomes:

$$\ell_g = \frac{4}{f^{2/3}} \tag{16}$$

when ℓ_g is the required gate length in μm for the FET to have useful gain at f GHz. The required gate length is inversely proportional to $f^{2/3}$.

The required gate lengths for 4-, 10-, and 20-GHz operations are 1.4, 0.9, and 0.5 μm, respectively. Figure 36 is a plot of ℓ_g as a function of frequency. The channel thickness T should be small compared with ℓ_g. If T is comparable to ℓ_g, the effective gate length will be much higher than the physical gate length ℓ_g as depicted in Fig. 37. Assuming that the fringe field at the gate edge has a circular equipotential plane, and that the radius of the equipotential plane equals the depletion depth at the drain side plus one-half of the depletion depth at the source side (Fig. 37), the effective gate length at the pinch-off condition is therefore:

$$\ell_{g\ \text{effect}} = \ell_g + 1.5\ T \tag{17}$$

If the channel thickness is equal to the physical gate length, $T = \ell_g$, the effective gate length is 2.5 times bigger than the physical gate length. It is desirable to keep T no bigger than 1/3 of ℓ_g. Assuming $\ell_g = 3T$, the channel

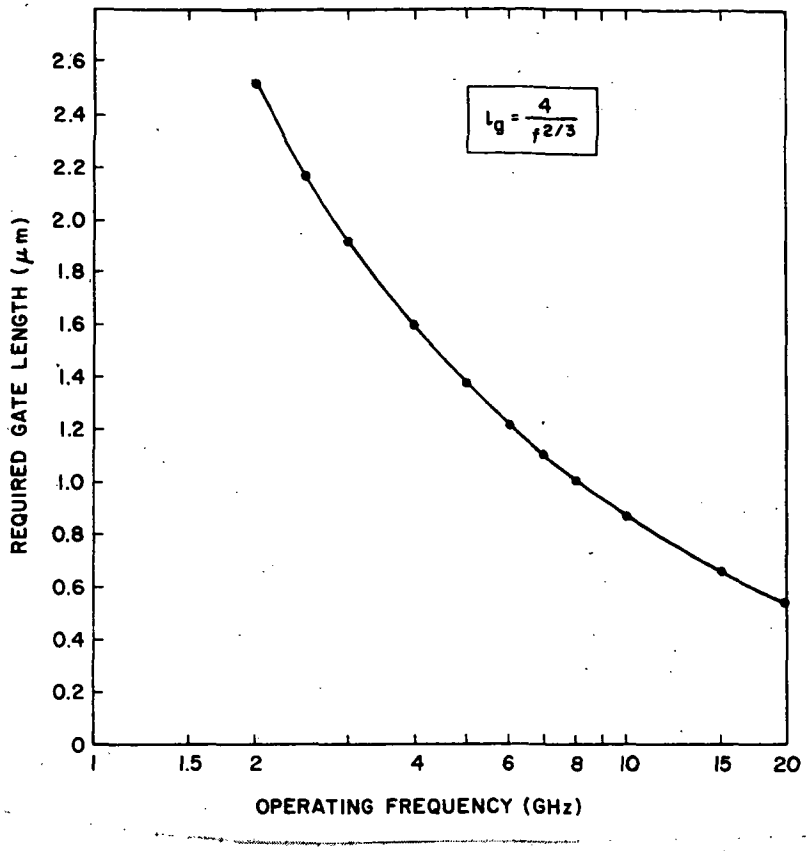

Figure 36. Required gate length as a function of operating frequency.

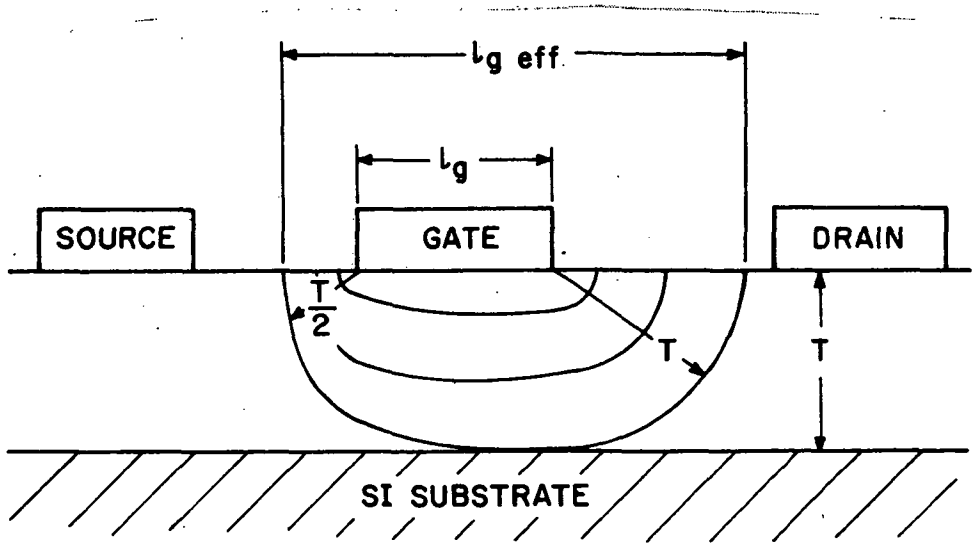

Figure 37. Effective gate length of an FET. $\ell_{g\ eff} \cong \ell_g + 1.5\ T$.

thickness T can be calculated for each frequency. This is also plotted in Fig. 36. The optimal nT product for power FETs is about 2.5×10^{12} cm^{-2}. Therefore, the carrier concentration n can be calculated. This is listed in Table 11. With the carrier concentration n known, the bulk breakdown voltage V_B of the Schottky-barrier gate and the pinch-off voltage V_P can be calculated. V_B and V_P are also included in Table 11. The instantaneous gate-to-drain voltage is roughly the sum of the dc drain bias voltage V_D, the gate bias voltage V_G, and the rf voltages on the drain and the gate. The dc gate bias voltage is roughly one-half the pinch-off voltage, $V_G = 1/2\ V_P$. The rf voltage is a function of the impedance matching at the gate and the drain side. Under certain matching conditions, the sum of the gate and drain rf voltages can be as high as the sum of the dc bias voltages [7]. For normal operating conditions, we can assume that the sum of the rf voltages is one-half the sum of the dc bias voltages. The maximum instantaneous voltage across the gate-drain terminal is:

$$\left|V_{gd}\right|_{max} = 1.5(V_D + \left|V_G\right|) \tag{18}$$

The dc gate bias voltage is usually set at one-half the pinch-off voltage V_P. In practical applications, where high reliability and long lifetime is required, it is desirable to keep $V_{gd\ max}$ below the bulk breakdown voltage V_B. Substituting $V_{gd\ max} = V_B$ and $V_G = 1/2\ V_P$, Eq. (18) becomes:

$$V_D = 0.67\ V_B - 0.5\ V_P \tag{19}$$

The drain bias voltage V_D as a function of frequency is also included in Table 11. In actual device operation, the electric field in the channel is nonuniform and there is a voltage drop in the source-gate region. Therefore, the gate breakdown voltage is different from the bulk breakdown voltage V_B. The values listed in Table 11 are, however, in reasonably good agreement with experimental observations. Hence, Table 11 can serve as a semi-quantitative design guideline. Even with the ability of tailoring the channel thickness T

7. F. Sechi, H. Huang, and B. Perlman, "Voltage and Current Waveforms in Power MESFETs Operating at Microwave Frequencies," Digest, ISSCC 1978, San Francisco, CA, Session THPM 13.4.

TABLE 11. GaAs FET DESIGN

$nT = 2.5 \times 10^{12} cm^{-2}$, $\ell_g = 3T$

Frequency, f (GHz)	2	4	8	10	15	20
Gate length, ℓ_g (μm)	2.52	1.59	1.0	0.86	0.66	0.54
n-layer thickness, T(μm)	0.84	0.53	0.33	0.29	0.22	0.18
Carrier concentrations, $n(cm^{-3})$	$3x10^{16}$	$4.7x10^{16}$	$7.6x10^{16}$	$8.6x10^{16}$	$1.1x10^{17}$	$1.4x10^{17}$
Schottky gate breakdown voltage V_B(V)	34	24	19	18	14	12
Pinch-off voltage V_P(V)	14	9	6	5.4	3.5	3
Estimated dc drain bias voltage V_D(V)	16	12	10	9	8	7

during device fabrication, the carrier concentration still needs to be controlled to within about 20% for a given frequency of operation. Because of the different carrier concentration profile at the n-layer/buffer layer interface with different reactors, the optimal value of n should be determined experimentally.

The pinch-off voltage of the FET is given by:

$$V_P = 1/2\ T^2\ \frac{ne}{\varepsilon} = 1/2\ (nT)^2\ \frac{e}{\varepsilon}\ \frac{1}{n} \text{ or } V_P\ \alpha\ \frac{1}{n} \tag{20}$$

Since the nT product, or the operating current, is usually kept constant, the pinch-off voltage is inversely proportional to n. This can be seen from Table 11. The device designed for high-frequency operation must have a lower pinch-off voltage than that designed for lower frequency.

The dc transconductance g_m is defined as:

$$g_m = \left| \frac{\Delta I_d}{\Delta V_G} \right| \tag{21}$$

Before the onset of velocity saturation, g_m is given by:

$$g_m = \left|\frac{\Delta I_d}{\Delta V_G}\right| \simeq \frac{ne\mu WT}{V_P} = \frac{2\varepsilon W}{nT}(n\mu) \qquad (22)$$

where W is the total gate width. When the nT is kept constant, g_m is proportional to the product of the carrier mobility μ and carrier density n.

The output power per unit gate width can be calculated from Eq. (13) and Table 11. For 10-GHz application, we have from Table 11, T = 0.3 μm, n = 8.3×10^{16} cm^{-3}, V_B = 18 V, V_P - 5.4 V, V_D = 9 V. The maximum drain rf voltage (Fig. 34) V_{max} can be calculated by the equation:

$$V_{max} = 2(V_D - V_S)$$

where V_S is the voltage at the onset of current saturation (Fig. 34), $V_S \simeq 2$ V. Hence, V_{max} = 14 V. Therefore, the output power per unit gate width is:

$$P = 1/8\ V_{max}\ neT\ V_m\Gamma = 5.6\ W/cm = 0.46\ W/mm$$

where $V_m = 10^7$ cm/s is the electron saturation velocity in GaAs and Γ = 0.8 is the degradation factor. We conclude that the power output is approximately 0.5 W/mm of gate width. The output power of a cell with four 150-μm gate stripes in parallel is therefore 300 mW. At 9 GHz, we have experimentally achieved an output power of 1 W from a 3-cell device. This corresponds to 0.56-mW/μm gate width. This is in fair agreement with theoretical calculations.

From the theoretical calculation and experimental results mentioned above, we conclude that the minimum gate widths required for cw 1-W and 4-W pellets are roughly 2000 μm and 8000 μm, respectively. Note that the gate width requirement is only one of the many important factors in device design. A device with a large gate width does not necessarily ensure high gain and high power output in X-band. Other factors such as device operating temperature, parasitic impedance, and phase incoherence can degrade both device output power and gain. We will now describe these factors in detail.

C. DEGRADATION FACTORS

1. Gate Width Limitations

It is desirable to make the gate of an FET as wide as possible to achieve high power. However, the gate-metallization resistance sets a limit on the

width of the gate, after which no further increase in output power is obtained with increase in gate width.

Figure 38 is a representation of an FET showing depletion layer capacitance $\bar{C}$, series charging resistor R, gate inductance L, and gate resistance R_g. High-frequency FETs are designed with the reactance of C greater than the gate inductive reactance. Thus, to the first order, the gate of an FET looks like an RC transmission line where a signal applied at one end both decays and changes phase as it travels down the line. The result is that for short gate widths, the input and output powers increase linearly with gate width, but for large gate widths input power never reaches the end of the gate, leaving the remaining region of the channel unmodulated.

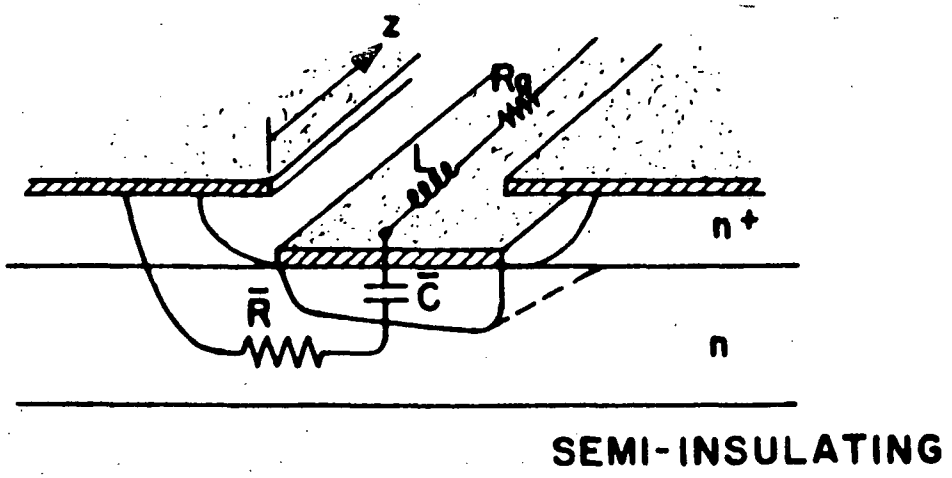

Figure 38. View of FET showing gate as a transmission line, indicating incremental unit.

With the same arguments that led to Eq. (4), the parasitic gate resistance is given by the expression

$$R_g = \frac{\rho_M W}{3 T_g \ell_g} \tag{23}$$

where W, ℓ_M, and T_g are the gate width, resistivity, and thickness, respectively. The power lost in the series gate resistance is, therefore

$$P_g = \langle I_{in}^2 \rangle R_g = \frac{1}{24} \frac{\omega^2 Q_o^2 \rho_M W}{T_g \ell_g} \tag{24}$$

Allowing this to equal half the useful power consumed in the channel leads to the condition:

$$W \leq \ell_g \left(2 \frac{T_g}{X_o} \frac{1}{en\mu\rho_M} \right)^{1/2} \tag{25}$$

For a 1-μm gate length, the width should be no larger than 200 μm. In this calculation we have used T_g = 0.5 μm, μ = 2500 $cm^2/V \cdot s$, $\rho_M = 4 \times 10^6$ ohm-cm, and X_o = 0.3 μm. In our current design, we use a gate stripe width of 150 μm.

2. Ohmic Contact Resistance

The source and drain contact resistances are also a source of power loss. The ohmic contact resistance R_{OH} is given by:

$$R_{OH} = \sqrt{\frac{\rho R_c}{T}} \Big/ W \text{ ohm} \tag{26}$$

where R_c is the specific contact resistance (ohm-cm^2) and T and ρ are the epitaxial layer thickness and resistivity, respectively.

We can now compute the allowable specific contact resistance. Allowing the power lost in the parasitic source resistance to equal half the useful power consumed in the channel leads to the following condition:

$$R_c \leq \left(\frac{2}{3} \frac{\ell_g}{4\mu n X_o} \right)^2 \Big/ \rho^+ \tag{27}$$

where $\rho^+ = 1/e\mu n^+ T^+$ is the sheet resistance of the n^+ capping layer. Numerical calculations show that it is easy to achieve the required contact resistance.

3. Parasitic Capacitance Effects

Consider the portion of the cycle which carries the depletion layer between profile 1 and profile 2. While no useful current modulation is obtained during this part of the cycle, charge must be circulated through the input circuit with a concomitant power loss. Since the voltage swings between forward

bias and pinch-off, the circulating current is rich in harmonics. We will estimate the power loss by assuming that the charge fluctuation is at the second harmonic.

$$I'_{in} = - \omega Q'_o \sin(2\omega t) \tag{28}$$

where $Q'_o = enW(T-X_o)\ell_g/2$, is the total charge between profile 1 and profile 2 in Fig. 33.

The total power lost in the parasitic resistance is given by

$$P_{INP} = \left[\langle I_{IN} \rangle^2 + \langle I'_{IN} \rangle^2 \right] R_P \tag{29}$$

where $\langle I_{IN} \rangle^2$ is the mean square current computed previously. The total input power becomes:

$$P_{INT} = P_{IN} \left[1 + \left(1 + \frac{\langle I'_{IN} \rangle^2}{\langle I_{IN} \rangle^2} \right) \right] R_P/R_{IN} \tag{30}$$

Thus, the input parasitics reduce the gain by the factor ξ, where

$$\xi = 1 + \left[1 + (T/X_o - 1)^2 \right] R_P/R_{IN} \tag{31}$$

An increasing T/X_o ratio corresponds to increasing nonuniformity in the profile under the gate. In a small-signal analysis, such nonuniformity effectively reduces the average drift velocity and thereby decreases the cutoff frequency ω_T.

4. Parasitic Source Inductance Effects

To evaluate the effect of a parasitic source impedance, consider the simplified schematic of an FET as shown in Fig. 39. The output conductance, feedback admittance, and internal channel resistance are neglected. We can write:

$$V_s = (I_g + I_d) Z$$

$$I_d = (V_g - V_s) g_m$$

$$I_g = (V_g - V_s) j\omega C$$

$$\therefore \quad Z_{IN} = V_g/I_g = - \frac{j}{\omega C} + \left[1 - \left(\frac{j g_m}{\omega C} \right) \right] Z \tag{32}$$

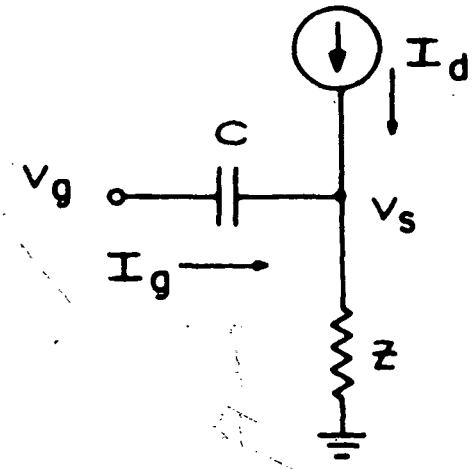

Figure 39. Circuit showing parasitic source impedance Z.

This equation shows that resistance in the source circuit has the same effect as resistance in the gate circuit. Equation (32) also shows that an FET transforms inductance in the source circuit into an equivalent resistance in the gate circuit. The multiplier, $g_m/(\omega C)$, the current gain, is on the order of unity at frequencies of interest. It is important to minimize the source inductance introduced by packaging. An effective solution is to flip-chip package the transistor. In this case, the sources are bonded directly to an rf ground plane through very short source posts. Thus the source inductance effect is negligible even up to K-band frequencies.

5. Numerical Example

To serve as a numerical example of the effect of the degradation factors described above, we will calculate the optimum nT product, and the gain as a function of frequency with gate length as a parameter. In order to simplify the calculation, we will consider two special cases for gate widths of 200 μm and 400 μm, respectively. The gate metal is assumed to have a resistivity of 4×10^{-6} ohm-cm and to be 0.5 μm thick.

Figure 40 shows the gain at 10 GHz for a device with 400-μm gate width and for various doping densities, assuming that channel thickness, biases, and circuit tuning have all been set for maximum gain. The parameter is gate length. One can see that the maximum available gain is relatively insensitive to doping density. With a 1.0-μm gate length, the optimum doping density is

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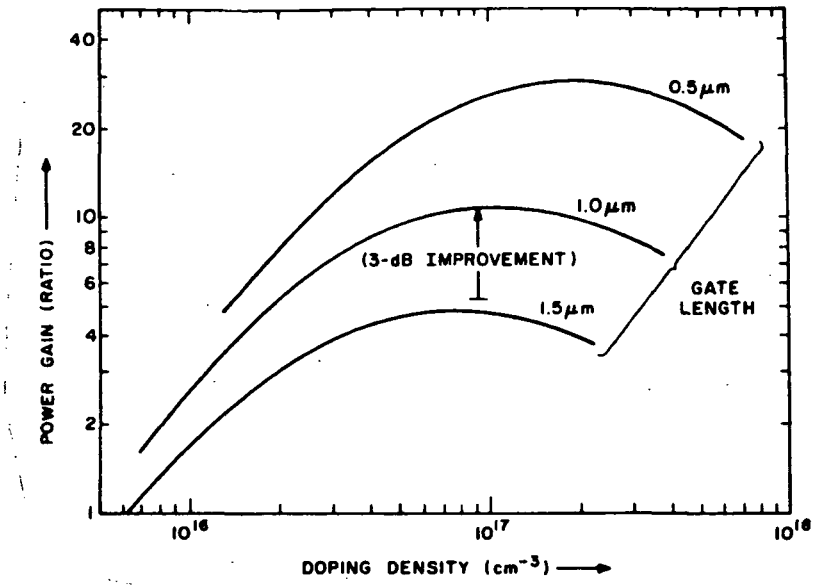


Figure 41. Maximum power gain vs doping for W = 200 μm at 10 GHz.

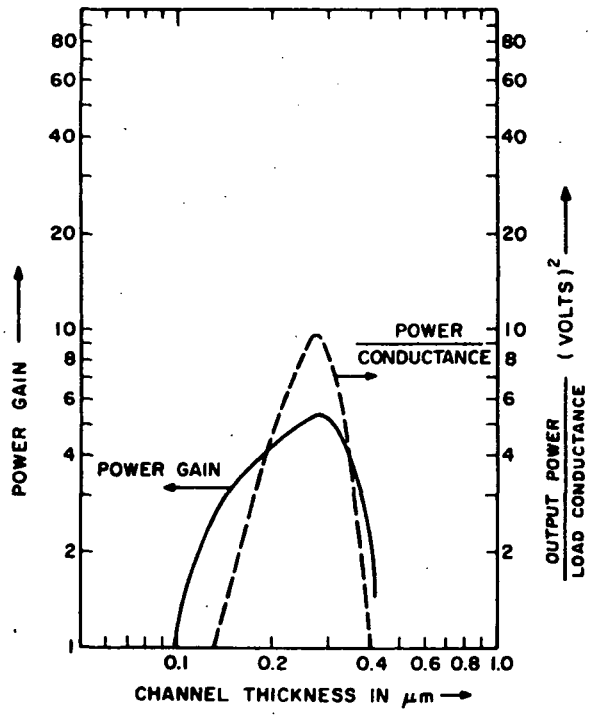


Figure 42. Gain and power/conductance vs channel thickness for $N = 9 \times 10^{16}$ cm^{-3} and $\ell_g = 1.0$ μm at 10 GHz with W = 400 μm.

D. FET PELLET DESIGN

We now have enough information for preliminary design of the 1-W and 4-W FET pellets required for this program. The two major results derived earlier, i.e., gate stripe width of less than 200 μm and output power of 0.5 mW/μm of gate width, will be used. A gate length of 1 μm will be chosen. The active layer carrier concentration of $8\text{-}10\text{x}10^{16}$ cm^{-3} will be used. Figure 43 is a schematic diagram of a unit cell of the FET pellet for 1-W output power at 10 GHz. We have chosen a stripe width of 150 μm and total cell gate width (source periphery) of 2.4 mm. From both theory and experimental results this cell is capable of an output power in excess of 1 W at 10 GHz. Since there are 16 gate stripes in parallel, we will call this 1-W design a 16-gate FET. In this design, the output power is proportional to the active area. Table 12 summarizes the FET design. These are advantages and drawbacks of this constant power per unit gate width design concept. In particular, since the dc input and rf output power density are nearly constant for all the geometries, the channel operating temperature is substantially constant for all the output power levels. Therefore, the operating lifetime is about the same for different types of FETs with different output powers. On the other hand, the device input and output impedances are inversely proportional to output power. Therefore, at each frequency band, there is a maximum gate width beyond which the device impedance becomes too low to match. In order to achieve an output power higher than this maximum gate width, partial impedance matching of individual cells before paralleling is needed. A different concept of increasing the output power is to increase the dc and rf voltages. This scheme is limited by the device breakdown voltage. Therefore, some basic studies of two-dimensional breakdown phenomena along different crystal orientation are required. There was no accurate theoretical model or any numerical computation to serve as design guidelines during the course of this program. Thus, only a limited effort was made to explore the means of increasing the device high-voltage capability beyond the limitation of bulk breakdown.

E. GaAs FET FABRICATION TECHNOLOGY

1. Introduction

Our major objective in pursuing programs on GaAs FETs has been to develop a technology which leads to high-performance, high-reliability devices and

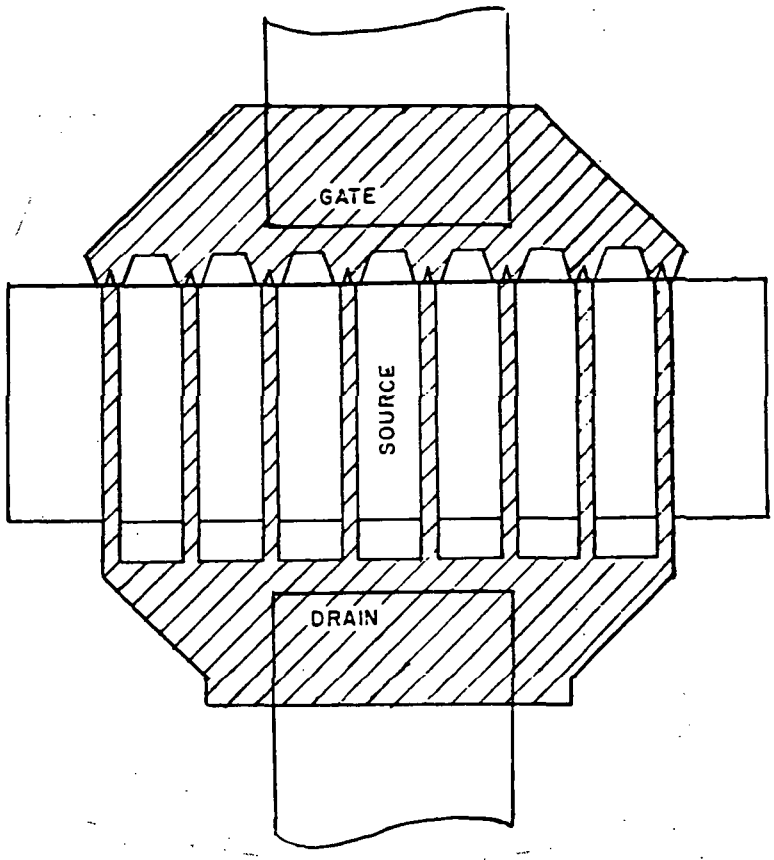


Figure 43. Schematic diagram of a 16G GaAs FET capable of 1-W output power. The chip size is 0.64 mm x 0.76 mm (0.025 in. x 0.030 in.).

TABLE 12. SUMMARY OF FET DESIGN

Parameter	8-gate	16-gate
Unit gate width (1μm)	150	150
Gate width per unit cell (μm)	1200	2400
Gate length (μm)	0.8-1.0	0.8-1.0
Design output power (W)	0.5	1.0

which can be ultimately adapted to large-scale production. We are currently producing devices by two different fabrication techniques. The first technique, a self-aligned gate process, was developed previously. This process makes use of modern microfabrication techniques such as ion-beam milling to avoid undercutting problems and result in almost a 1:1 photoresist pattern to actual device geometry ratio. As first developed this technique had no convenient method of

compensating for the active layer thickness variations commonly encountered in epitaxially grown wafers. During this contract period a method was developed to improve yield and device uniformity by use of an anodic thinning procedure to automatically compensate for epitaxial layer thickness variations.

This second method of device fabrication makes use of lift-off metallization techniques to produce an aligned-gate device. This process includes automatic adjustment of the epitaxial layer thickness by electrolytic anodization to achieve an active layer with uniform nT product. This material uniformity will result in improved rf performance of high-power FETs.

2. Self-Aligned Gate Fabrication Technology

a. Outline of Basic Fabrication Process

Figure 44 is a schematic cross section of a typical GaAs power FET. Figure 45 is a scanning electron micrograph (SEM) showing a typical 8-gate FET pellet. The pellet size is 0.056x0.056x0.018 cm^3 (0.022x0.022x0.077 in^3). Each cell consists of four 8-gate stripes in parallel. The gate length is nominally 1 μm and the gate stripe width is 150 μm corresponding to a cell source periphery of 1200 μm. Each cell has 5 sources and 4 drains.

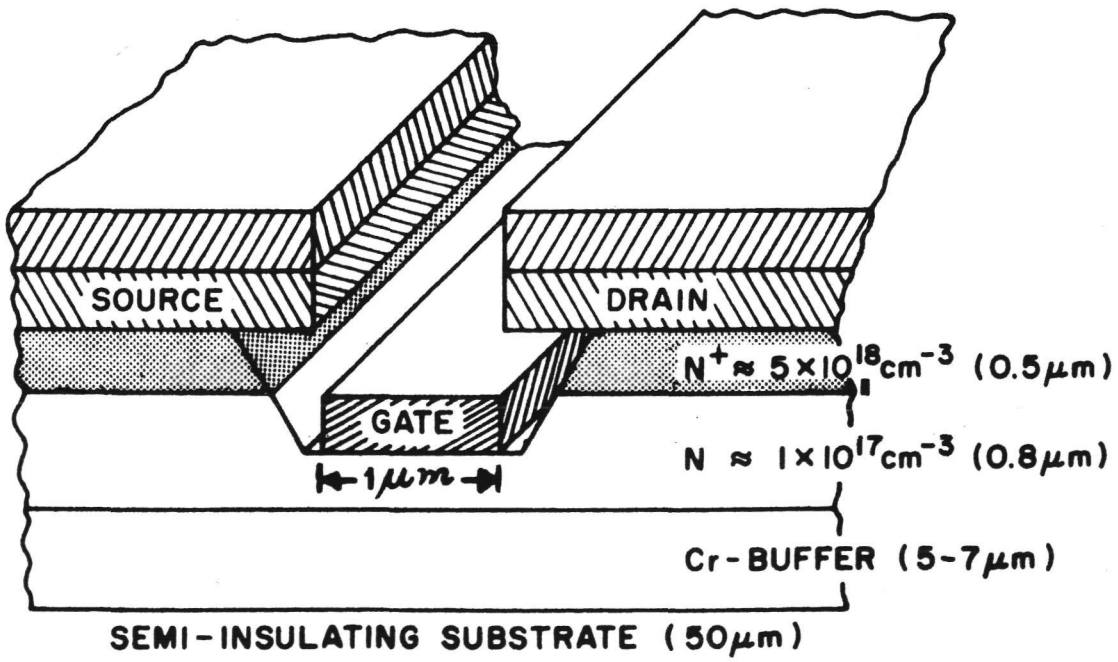


Figure 44. Schematic cross section of RCA GaAs FET.

Device fabrication starts with an n^+-n-SI GaAs wafer grown as described previously. The wafer may or may not have a buffer layer. Since a buffer

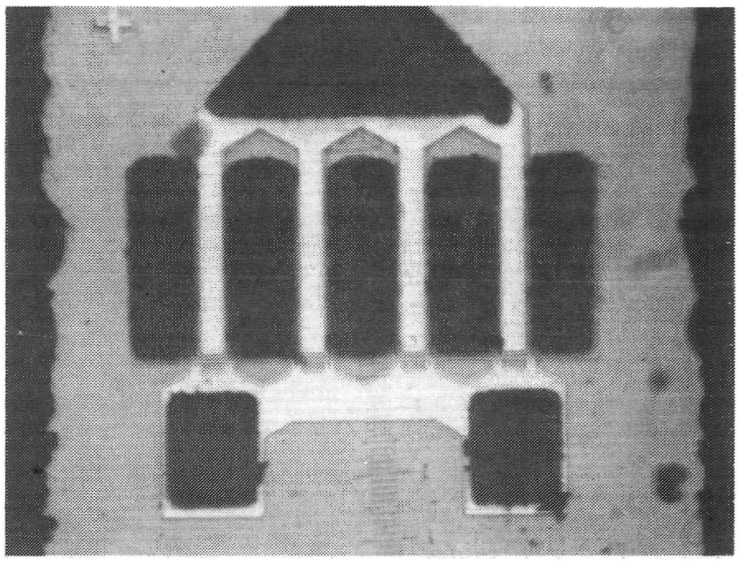


Figure 45. An 8-gate FET pellet.

layer does not modify the fabrication process, we will ignore its presence in our description. This process can be described with reference to Fig. 46. Conventional photolithographic techniques such as contact masking are used throughout. Standard positive working photoresists are used to define metallization patterns, and the metal itself is used to mask in order to form the channel and isolate the various device elements. The salient steps are:

(1) The source and drain areas are selectively metallized with AuGe/Ni ohmic contacts. This step is followed by titanium-platinum and gold metallization.

(2) Photoresist patterning is used to define the mesa. Mesas are formed using ion-beam etching (IBE).

(3) A second photoresist pattern is defined which splits mesas into alternating source and drain electrodes. Openings (i.e., channels) in the photoresist between adjacent electrodes are about 1 μm.

(4) The channels formed in the photoresist are cut using IBE down to the n-layer of the wafer. During IBE, source-to-drain saturation current (I_{DS}) is monitored and the process stopped when the channel thickness is appropriate for good FET performance. Typically, the value of I_{DS} at this point is 5 to 15 A/cm of gate width.

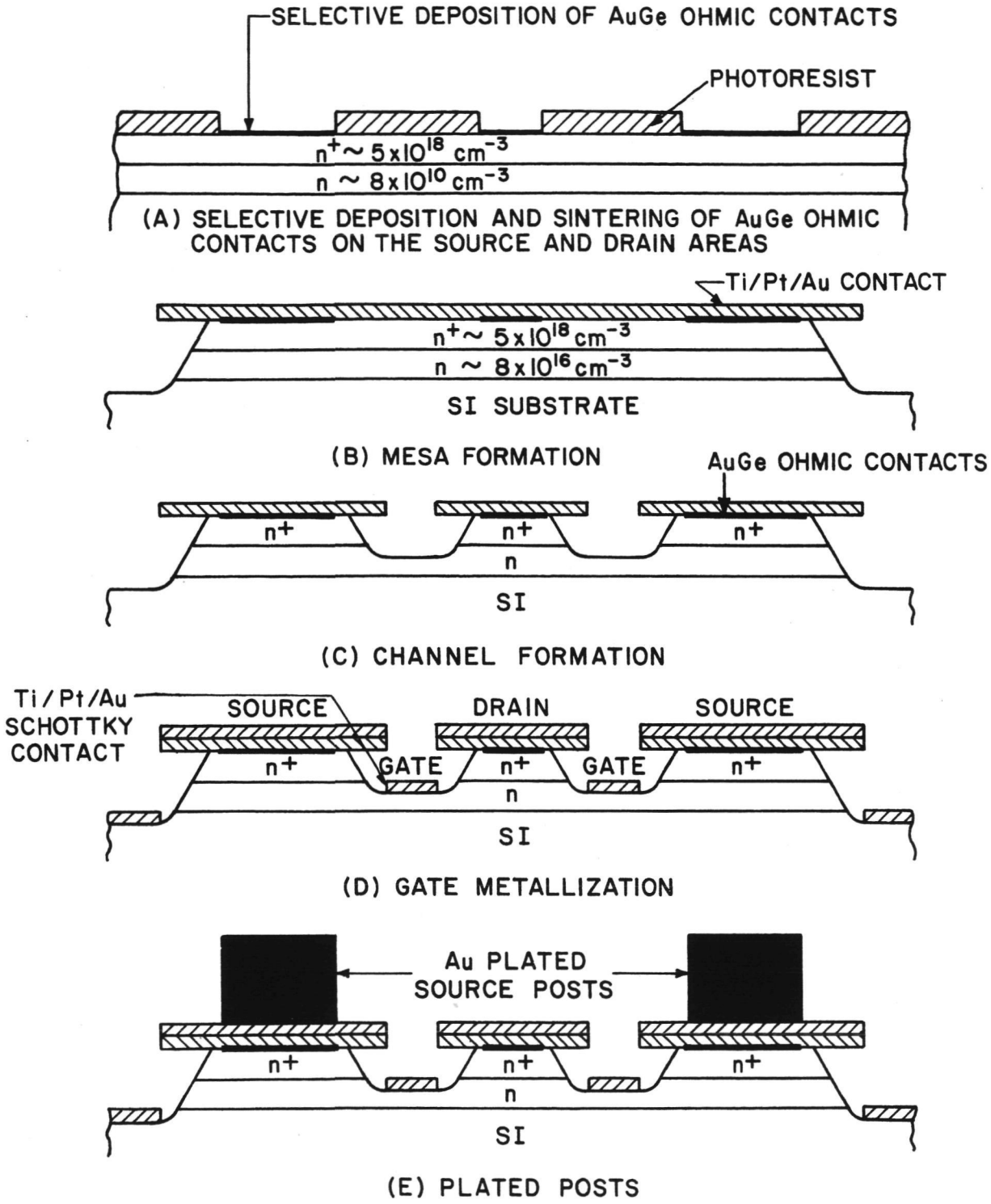


Figure 46. Process diagram for the self-aligned gate process.

(5) A chemical "touch-up" etch is used to give enough undercut to prevent shorting in later steps (Fig. 46).

(6) A second Ti/Pt/Au evaporation places the gate stripes into the channel formed by earlier steps. Since the source and drain pads are undercut, there is no shorting of gate to either pad. Also because the material in the active channel is lightly doped ($\sim 10^{17}$ cm^{-3}), the titanium forms a Schottky-barrier contact (Fig. 46d).

(7) Finally, a photoresist pattern is defined for the gate bonding pad. Excess metal is removed by IBE, and, after cleaning, devices are ready for dc testing.

The n^+-layer thickness of the wafer is carefully chosen to allow gate metallization thicknesses of between 4000 and 6000 Å. About 5000 Å of gate metallization is desirable to decrease the effects of gate metallization resistance. Excessive gate metallization can lead to short circuits between the gate and source or drain contacts.

The smallest gate length that can be achieved by this process is that set by the resolution of the photomask. Since ion-beam etching does not undercut, we can obtain 1:1 mask resolution to metal definition ratio. We have obtained excellent photomasks with 1-μm gate stripes and with these have obtained gate lengths just under 1 μm (Fig. 47).

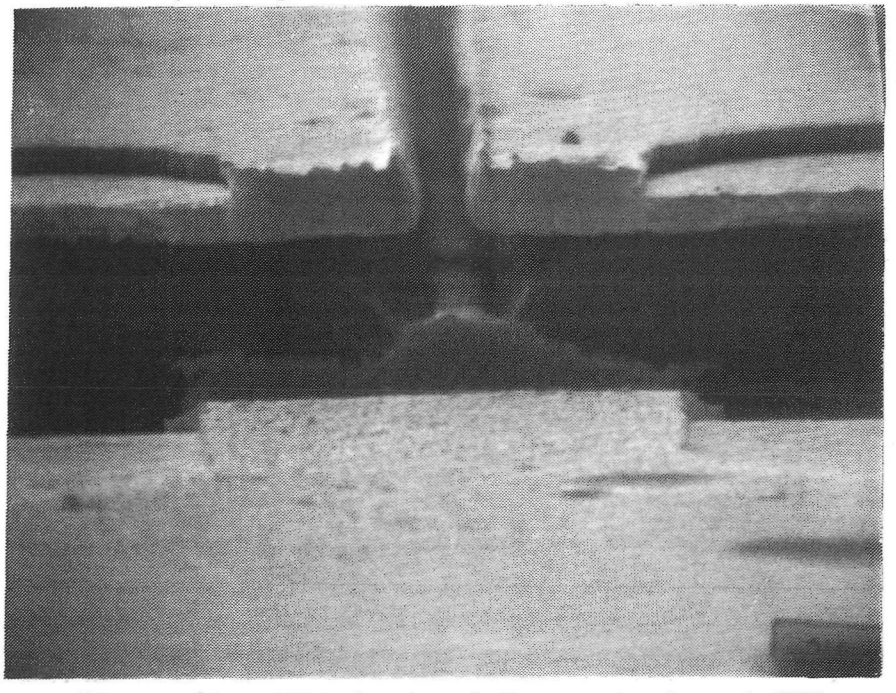


Figure 47. SEM showing 0.5-μm gate length FET.

b. Process Development

During the course of this contract we conceived of a method of employing the anodic oxidation and oxide removal technique to compensate for epitaxial layer thickness variations on wafers to be used for self-aligned gate fabrication. Standard anodization and oxide removal cycling to completion in the dark is not suitable because this reduces the active layer to the pinch-off thickness (approximately 0.4 μm for $1x10^{17}$ cm^{-3} material) while the self-aligned gate process requires active layers greater than 1 μm thick. The basic concept is quite simple. If a moat is chemically etched around a region of a wafer and then the wafer is thinned by the anodic oxidation process, the region surrounded by the moat will stop being thinned when the moat reaches the pinch-off thickness. Once the recessed moat area surrounding the region reaches the pinch-off thickness, the high resistance depletion layer of the moat disconnects the surrounded region from the applied bias of the electrolytic cell and no further oxidation takes place.

This concept can be used in a straightforward manner if the active layer consists of only an n-layer. A grid pattern can be used to etch a recess around each device area. The depth of the recess will determine the final thickness of the active layer. For example, if the doping density is such that the pinch-off thickness is 0.4 μm and one wanted to end up with an n-layer 1.5 μm thick, the n-layer must be grown slightly thicker than 1.5 μm and the depth of the recess should be 1.1 μm. After etching the grid recess, the photoresist is removed so that the entire surface of the wafer will grow an anodic oxide. Each oxidation and oxide removal cycle removes an equal thickness from the device area and the moat until the moat area is thinned to 0.4 μm. Since the moat was originally etched to a depth of 1.1 μm, the thickness of the n-layer in the device area is 1.5 μm. Sections of the wafer with thicker epitaxial layers will continue to be thinned until the moat everywhere is reduced to the pinch-off thickness and all the device areas are 1.5 μm thick. Figure 48 illustrates this process at an intermediate point in the anodic thinning process. Each square is an active device area. The shades of black are caused by the presence of oxide layers of different thicknesses. The squares on the lower right corner have no oxide because the moat surrounding them has reached the pinch-off thickness.

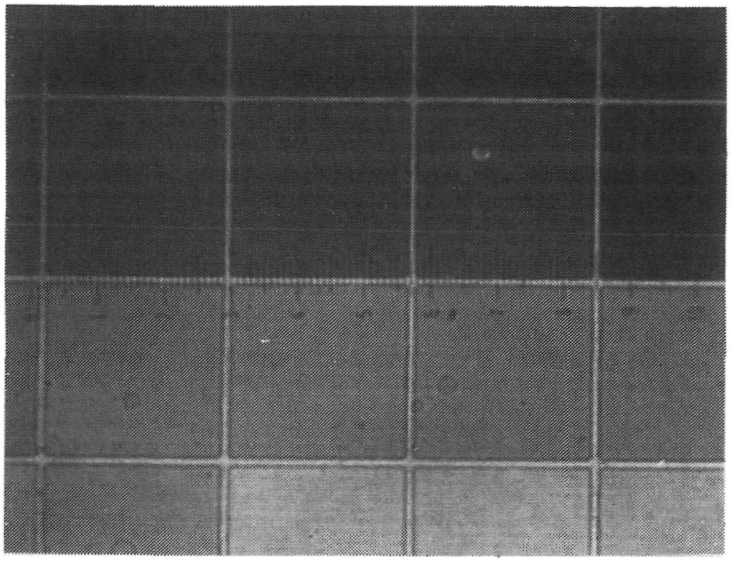


Figure 48. Wafer undergoing anodic thinning after an initial grid etch of 1.2 μm. Each square represents an area where one device will be located. The shade of gray of each device area is related to the thickness of the oxide grown during anodic oxidation.

This technique is complicated by the presence of an n^+ capping layer. The difficulty is that the oxide growth rate is greater for the n^+ layer than the n^- layer of the moat because of the difference in avalanche breakdown voltage. A difference of 10 V in the breakdown voltage would result in the removal of 150 Å more from the device area than is removed from the moat region during each oxide growth-oxide stripping cycle. If the moat region around a given device area reaches the pinch-off thickness after N oxidation cycles, the active device area thickness would equal the pinch-off thickness plus the moat etch depth minus 0.015N μm. That is, the final device area thickness becomes a function of the number of oxidation cycles. The wafer uniformity can still be improved even with an n^+ capping layer, but the number of oxidation steps must be restricted.

There is one problem with this technique even when the wafer consists of only an n layer. The initial chemical etch should not be so deep that the material left in the grid recess is less than the pinch-off thickness. To overcome this limitation a method was developed to perform anodization and oxide removal with the grid pattern photoresist masking layer in place. This

allows one to anodically thin the grid recess area with the device areas protected until the grid in the thinnest section of the wafer reached the pinch-off thickness. Removal of the photoresist at that point allows for controlled thinning of the thicker sections of the wafer by the anodization and oxide removal process. An electrolyte consisting of deionized H_2O adjusted to a pH of 3 with H_3PO_4 was found not to attack the positive photoresist used to mask the device areas. An etchant consisting of phosphoric acid plus water in a ratio of 1 to 30 by volume was found to be satisfactory for removing the anodic oxide without attacking the photoresist layer.

In addition to improving the uniformity of the epitaxial layer this grid recess and anodic thinning process also allows one to determine what thickness of GaAs must be removed from the gate channels by the combination of ion-beam milling and the touch-up chemical etch [Fig. 46(c)]. Since the grid recess ends up at the pinch-off thickness and the gate should be placed just slightly deeper than the pinch-off thickness, the step height between the top of the active device area and the level of the grid recess is approximately the thickness of GaAs to be removed from the channel. In order for this thickness measurement to be of value the ion-beam milling rate in the device channel must be known accurately and the milling rate should be fairly constant from wafer to wafer.

The first wafers processed using the grid depth as an ion-beam milling guide seemed to reach the desired value of the source-to-drain saturation voltage at a depth much less than expected. This was found to be caused by a phenomenon known as trenching, characteristic of ion-beam milling at normal incidence. Enhanced milling at the edge of the masked region produces a depression or trench which is deeper than the area farther away from the edge of the masked region. The trenching effect is clearly shown in Fig. 49, which is an SEM of a cleaved section of the gate area of the test pattern used to measure the milled depth of the gate channel. The left side of the picture is the gate region of the device and the right side is the source metallization. The photograph shows a trench next to the edge of the source approximately 0.3 μm deeper than the 1.8-μm depth of the main section of the gate. When the actual device gate channel was examined, the gate channel was found to be substantially deeper than the trench seen on the test pattern device. The gate recess was approximately 2.8 μm as shown in Fig. 50. Apparently, for a very

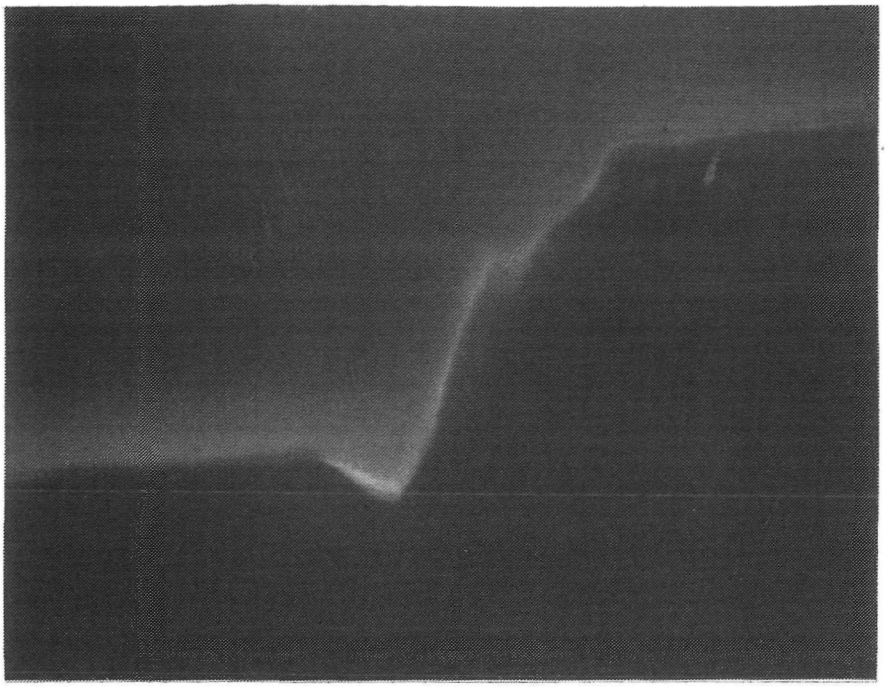


Figure 49. SEM of the gate region of the long gate FET test pattern device. Wafer C722. Magnification: 20,000X.

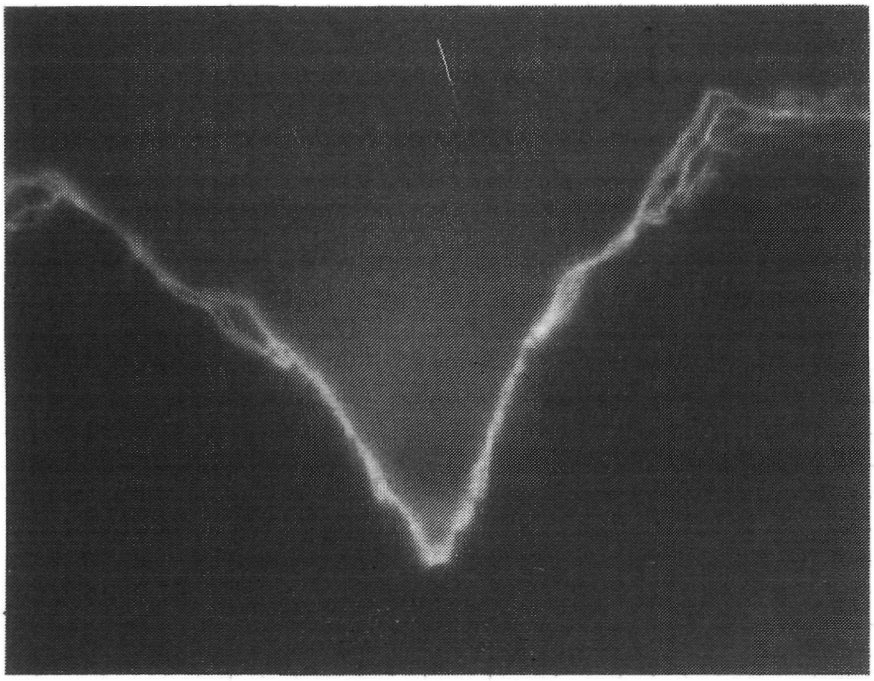


Figure 50. SEM of the gate region of a power device. Wafer C722. Magnification: 20,000X.

narrow opening the trenching effects from both edges are combined to enhance the milling rate. This is not a fundamental limitation on the grid recess technique of preparing wafers for ion-beam milling. The trenching effect can be accounted for by increasing the assumed milling rate, as long as the milling rate is constant from wafer to wafer. Even if the milling rate is not predictable, the grid recess thinning process is still of value in improving the thickness uniformity of the epitaxial layer. During ion-beam milling, the milling time can be determined in the standard way by monitoring the source-to-drain saturation current (I_{DS}).

3. Aligned-Gate Fabrication Technology

During the course of this program an aligned-gate process has been developed. Although excellent device results have been achieved with the self-aligned gate process, there were four reasons for investigating an alternate technique involving an aligned gate produced by a lift-off process. First, in the self-aligned gate device the effective gate-to-source and gate-to-drain spacing is identical. Ideally one would like to have the gate located closer to the source to minimize the parasitic source-to-gate resistance and increase the gate-to-drain separation to enhance the gate-to-drain breakdown voltage [8]. This can be achieved in an aligned-gate device by simply designing the gate mask so that the gate is located closer to the source than to the drain.

A second reason for the aligned-gate process is that the self-aligned gate process had no automatic or easy way of compensating for the thickness variations of the epitaxial layer inherent in the epitaxial growth process. In the aligned-gate process, the epitaxial layer can first be thinned to a uniform thickness by anodic oxidation and oxide removal cycling to completion [9]. This process is self-limiting, automatically stopping at the pinch-off thickness (thickness of the depletion layer at avalanche breakdown).

The third reason for pursuing an aligned-gate process is to avoid the use of ion-beam milling. In the self-aligned gate process, ion-beam milling is used to create the gate channel because it does not produce the lateral undercut

8. J. A. Turner, A. J. Waller, R. Bennett, and D. Parker, "An Electron Beam Fabricated GaAs Microwave Field Effect Transistor," 1970 Symp. on GaAs, p 234-239.
9. D. L. Rode, B. Schwartz, and J. V. DiLorenzo, "Electrolytic Etching and Electron Mobility of GaAs for FETs," Solid State Electron. 17, 1119 (1974).

of chemical etching techniques. It can therefore maintain the gate length defined in the photoresist layer. The surface damage resulting from ion-beam milling may result in defects which diffuse into the GaAs. Defects diffused to a depth of about 2000 Å have been reportedly produced by ion-beam milling with 500-eV Ar [10]. Ion-beam milling through metal layers may also result in nonuniform removal of material. It has been reported that in ion-beam milling of polycrystalline metal layers, material is removed preferentially at grain boundaries [11]. Once the metal layer is milled away, the resultant surface roughness is passed on to the underlying material. For the self-aligned gate device this can result in a nonuniform channel and decrease the device efficiency. The damaged layer from ion-beam milling can be eliminated by the subsequent chemical etch of the gate channel, but surface roughness may not be eliminated. The aligned-gate process does not require ion-beam milling at all.

Finally, a thick epitaxial layer is required for the self-aligned gate process. To achieve thick gate metallization the normal thickness of the epitaxial layer is 1.25 to 1.5 μm. The ion-implantation equipment presently being used is limited to an implant depth of approximately 0.25 μm. Thus the self-aligned gate process cannot be used to fabricate devices from currently available ion-implanted wafers.

a. Outline of Basic Fabrication Process

The basic design of the aligned-gate device is identical to the self-aligned gate device except for the source/drain level and the gate level. The source/drain mask was designed with a 4-μm-long channel. The gate mask was designed to produce a 1-μm gate, 1 μm away from the edge of the source.

The original device fabrication sequence is illustrated in Fig. 51. The starting wafer consists of a semi-insulating GaAs substrate with an n layer grown by vapor-phase epitaxy or produced by ion-implantation and annealing.

10. M. Kawabe, N. Kanzaki, K. Masuda, and S. Namba, "Effects of Ion Etching on the Properties of GaAs," Applied Optics 17, 2556 (1978).
11. H. Dimigen and H. Lüthje, "An Investigation of Ion Etching," Philips Tech. Rev. 35, 189 (1975).

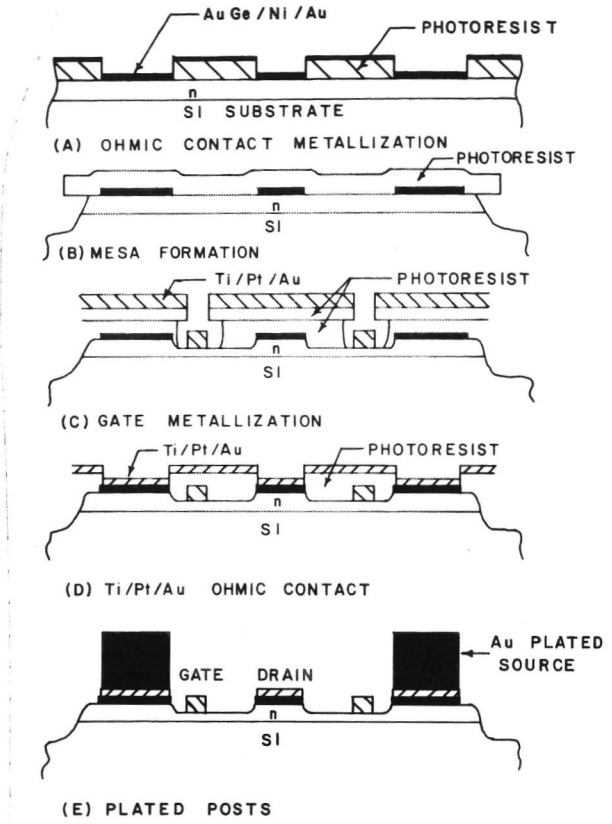


Figure 51. Process diagram for the aligned-gate process.

Standard positive working photoresists are used throughout the process. The principle processing steps may be summarized as follows:

(1) The active device layer is first thinned by anodic oxidation and oxide removal cycling to completion. This reduces the active layer to the pinch-off thickness.

(2) The source and drain areas are metallized with AuGe/Ni/Au by the lift-off technique. Sintering at 450°C for ∿1 minute is used to produce ohmic contacts.

(3) Device mesa regions are defined in photoresist and chemical etching is used to isolate individual devices.

(4) A chemical etch is used to adjust the saturation current to the appropriate value for good device operation.

(5) A double photoresist layer lift-off technique is employed to define the gate. The bottom photoresist layer is spun on, prebaked, and given a blanket exposure but not developed. Next, a thin, semitransparent layer of titanium (~80 Å) is evaporated to allow the top photoresist layer to be applied. The exposed titanium layer is etched away and then the bottom photoresist layer is developed. After evaporation of the Ti/Pt/Au gate metallization, the photoresist is removed by organic solvents as in the conventional lift-off technique.

(6) A Ti/Pt/Au metal layer is deposited by the lift-off technique on the source and drain to act as a diffusion barrier and to lower the drain spreading resistance.

(7) Finally, a thick photoresist layer is patterned for gold plating of bonding bumps on the sources, drain pad, and gate pad areas.

b. Aligned-Gate Process Development

During the course of the project, some modifications were made to this basic aligned-gate process to overcome the problems of poor gate-metal adhesion, high saturation voltage, and low source-to-drain breakdown voltage.

The gate-metal adhesion problem was solved by an initial evaporation of a thin titanium layer over the entire substrate. Before any photoresist for the gate lift-off is applied to the sample, the wafer is subjected to the same cleaning sequence given to self-aligned gate wafers prior to the gate evaporation step. The wafer is then loaded immediately into the electron-beam evaporator system. While under vacuum, the wafer is heated to 300°C and then cooled to 120°C for an evaporation of a 1000-Å-thick layer of titanium. Next, the normal two-layer photoresist method is followed and gate pattern is formed in the photoresist. Immediately prior to depositing the gate metal, the sample is briefly etched in a titanium etchant to remove a small portion of the underlying titanium to expose a fresh layer. The resulting photoresist profile is shown in cross section in Fig. 52. The Ti/Pt/Au gate metal is evaporated with no intentional substrate heating. The undercut photoresist profile allows a relatively thick gate metallization to be deposited. The gate metallization can be nearly as thick as the bottom photoresist layer without causing any difficulty. Good adhesion is obtained between the evaporated titanium and the freshly etched titanium surface. Careful surface cleaning and vacuum

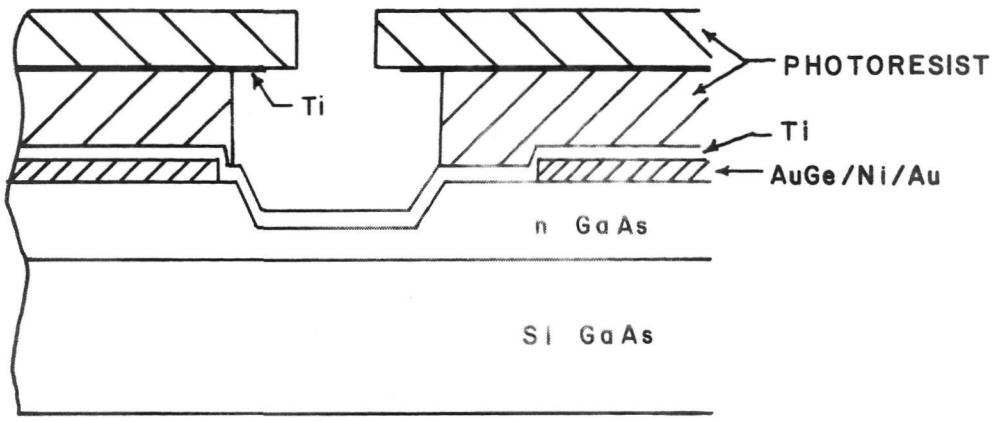


Figure 52. Schematic cross section of aligned-gate device prior to gate-metal evaporation.

baking produced good adhesion between GaAs and the original titanium layer. Bond pull strengths up to 6.5 grams were measured for 1-mil gold wires bonded between adjacent gate pads. After the lift-off process is completed by removing the photoresist in organic solvents, the original titanium layer is removed with a chemical etchant. By carefully controlling the etching time, the lateral etching of the titanium can be used to reduce the gate length, producing a "T" shaped gate, as illustrated in Fig. 53. Devices fabricated in this manner have been able to survive the flip-chip bonding procedure without failure of the gate-metal adhesion.

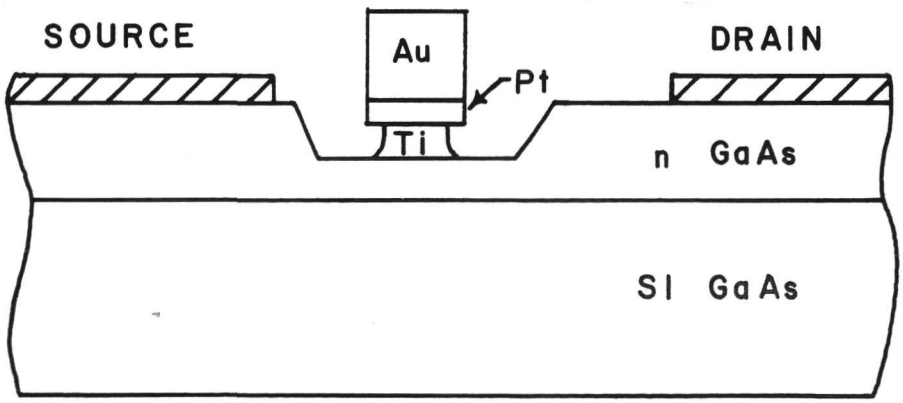


Figure 53. Schematic cross section of aligned-gate device after gate lift-off.

To produce high-power devices it is important to achieve as high a source-to-drain breakdown voltage as possible and simultaneously as low a value of

saturation voltage as possible. Devices fabricated by the original aligned-gate process normally showed low source-to-drain breakdown voltages (typically 7 to 8 V) and relatively high saturation voltages (2.5 to 3.5 V). Recent publications have reported that high source-to-drain breakdown voltage can be achieved by means of a recessed gate structure [12,13] and/or n^+ material under the source and drain [14]. Both an n^+ layer under the source and drain and a recessed gate structure will also help reduce the parasitic source-to-gate resistance and lower the saturation voltage.

A modification of the anodic thinning process was developed that allows one to leave thicker layers of GaAs under the source and drain regions while simultaneously thinning the active channel area to the pinch-off thickness. The basic modification to the anodic thinning process consists of first etching the channel and area outside the source and drain regions to a depth equal to the extra thickness desired in the source and drain regions. It is important that the phototresist pattern used for etching is such that each device is totally surrounded by a recessed area. Following the recess etching, the photoresist is removed, and the wafer is thinned by the anodic oxidation-oxide removal method until no further oxide will grow in the dark. One would expect the initial thickness difference between the source-drain and channel areas to vanish when the epitaxial layer is thinned everywhere to the pinch-off thickness. This does not occur because the source and drain regions of each device are surrounded by an area at the same active layer thickness as the etched channel. When the device channel reaches the pinch-off thickness, this surrounding area is also at the pinch-off thickness so that the source and drain regions are isolated from the voltage of the electrolytic cell by a high resistance depletion region. Therefore, the anodic thinning process stops for each device when the recessed region surrounding that particular device reaches the pinch-off condition. This technique has proved successful

12. T. Furutsuka, T. Tsuji, and F. Hasegawa, "Improvement of the Drain breakdown Voltage of GaAs Power MESFETs by a Simple Recess Structure," IEEE Trans. Electron. Devices ED-25, 563 (1978).
13. C. Tsironis, "Influence of Epilayer Properties on Breakdown Voltage and Noise Behavior of GaAs MESFETs," Revue De Physique Appliquie 13, 761 (1978).
14. W. C. Niehaus, H. M. Cox, B. S. Hewitt, S. H. Wemple, J. V. DiLorenzo, W. O. Schlaner, and F. M. Magalhaes, "GaAs Power MESFETs," Inst. Phys. Conf. Ser. No. 336, 1977, p 271.

even when the active device layer is capped with an n^+ layer. When an n^+ layer is used, the thickness of the n layer and the depth of the chemically etched recess must be chosen with some care to ensure that all of the n^+ layer is not removed during the anodic thinning process. Figure 54 shows a device from a wafer anodically thinned after a 0.5-μm channel recess was etched. Note that the drain connection to the grid was also chemically etched to completely surround the device with material etched to the same depth as the gate channels. Figure 55 shows a magnified view of the channel region after ohmic contacts were deposited and sintered and the mesa defined by chemical etching.

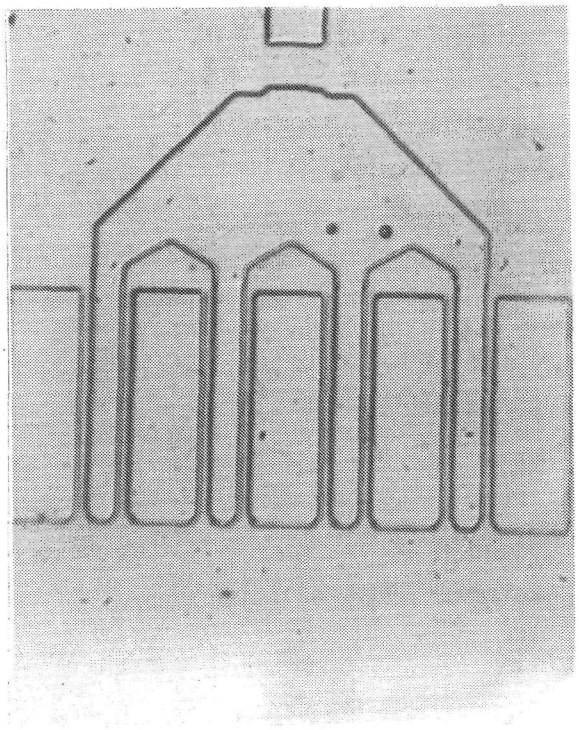


Figure 54. Micrograph of an aligned-gate device anodically thinned after a 0.5-μm channel recess was etched.

The improvement in source-to-drain breakdown voltage caused by the gate recess was clearly demonstrated by breakdown voltage measurements on ungated devices. To compare the effect on source-to-drain breakdown voltage of the n^+ layers, a companion wafer with only an n layer was processed also with a 0.5-μm gate recess. Since the gate mask used to define this recess region is designed to place the gate closer to the source than to the drain, the resultant recess edge is located quite close to the edge of the source. After forming the

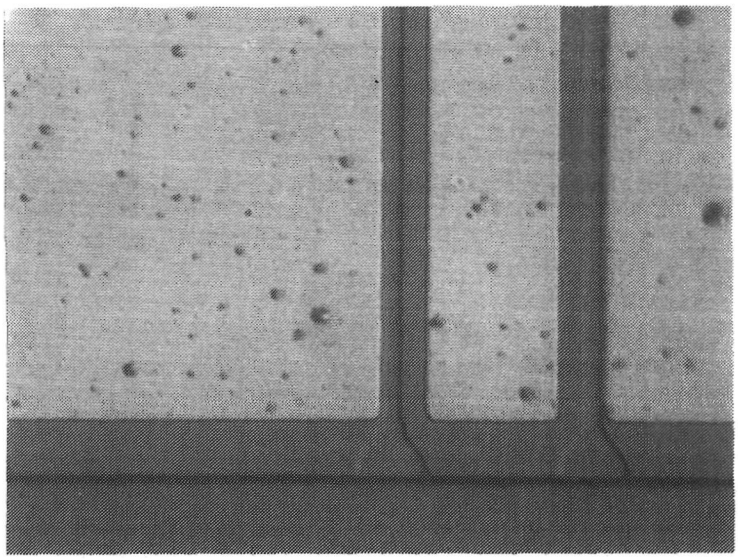


Figure 55. Micrograph of device channel area after ohmic contacts were produced and the mesa was defined by chemical etching.

ohmic contacts and mesa etching to isolate devices, the source-to-drain breakdown voltage was determined with a transistor curve tracer. Many devices on both the wafer with an n^+ contact layer (B281) and that with only an n layer (D241) showed asymmetrical source-to-drain I-V characteristics. Microscopic examination revealed that asymmetrical I-V characteristics appeared to correlate with devices which had source metallization extending into the gate recess.

The source-to-drain breakdown voltage was measured using a transistor curve tracer in the pulse mode with 80-μs pulses. The devices typically showed a higher breakdown voltage with the drain positive than with the source positive. The test results are shown in Fig. 56 for a typical device from the n layer wafer D241. The upper right quadrant (drain positive, normal polarity for device operation) was traced out first, showing no breakdown up to 12 V applied bias. The lower left quadrant (source positive) was then traced out for the device using the pulse mode and a time exposure to record the breakdown point. Breakdown occurred at approximately 7 V. The physical location of the point of breakdown for this device, examined with an optical microscope is shown in Fig. 57. The fact that the breakdown occurred far from the ends of the channel tends to rule out shape differences between the source and drain configuration as the cause of the asymmetry in breakdown voltage.

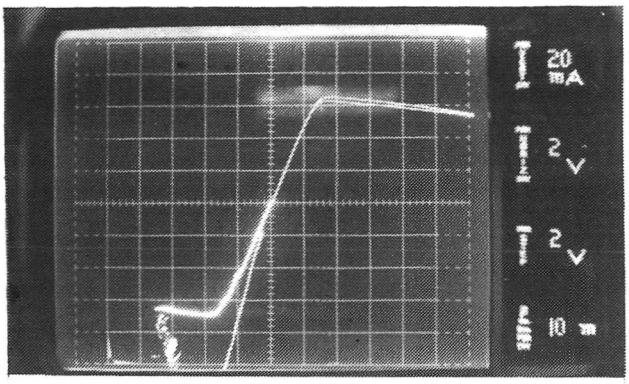


Figure 56. Source-to-drain breakdown voltage for wafer D241, n-layer wafer with 0.5-μm gate recess. Upper right quadrant: drain positive, breakdown > 12 V. Lower left quadrant: source positive, breakdown $\sim$ 7 V.

Figure 57. Optical micrograph of breakdown site (dark spot in channel) of device on wafer D241.

A similar type of source-to-drain breakdown measurement was performed on wafer B281 to see the effect of an n^+ layer. The results are shown in Fig. 58. The breakdown voltage shows the same asymmetry obtained on wafer D241. The

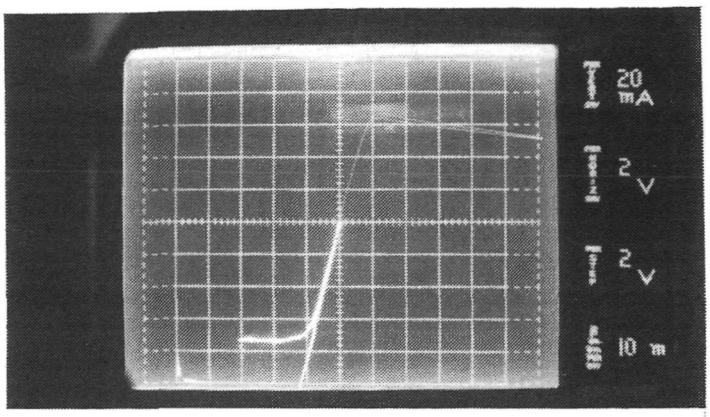


Figure 58. Source-to-drain breakdown voltage for B281, wafer with n^+ capping layer and 0.5-μm gate recess. Upper right quadrant: drain positive, breakdown > 12 V. Lower left quadrant: source positive, breakdown $\sim$ 7 V.

presence of n^+ material under the source did not increase the breakdown voltage (source positive, lower left quadrant of Fig. 58) when the edge of the source metal extended beyond the edge of the recess. The source-to-drain breakdown voltage with the drain positive was again greater than 12 V. The benefit of the n^+ layer can be seen in the improved saturation voltage V_{sat}. V_{sat} was approximately 2 V for B281, whereas V_{sat} for the n layer wafer was approximately 3 V. It appears that the n^+ layer is not necessary to achieve high source-to-drain breakdown voltage. This is in agreement with the findings of Furutsuka et al. [12]. The n^+ contacts are, however, beneficial in achieving low specific contact resistance and minimizing the saturation voltage.

Figure 59 shows the I-V characteristics of a completed device with a 280-μm-wide channel from wafer D241. As shown, the device exhibited a source-to-drain breakdown voltage of more than 15 V with a positive bias on the drain.

In addition to the above process modifications for processing epitaxial layer wafers, several processing changes were investigated for processing ion-implanted wafers. Due to the 250-keV energy limitation of our implantation equipment, the implanted layer depth is barely sufficient for fabrication of

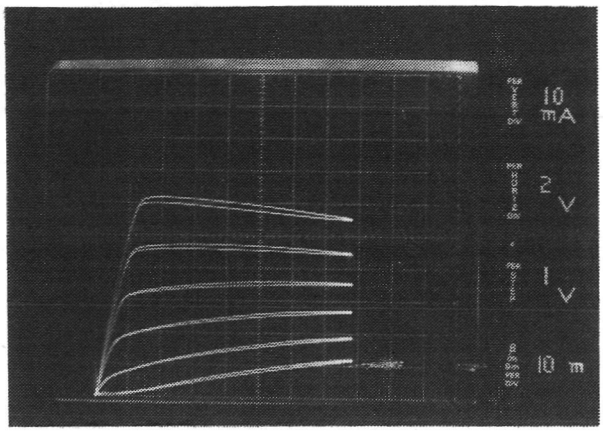


Figure 59. I-V characteristics of 280-μm-wide device on wafer D241. Source-to-drain breakdown > 15 V.

power FETs. The ion-implanted wafers as received were therefore similar to epitaxially grown wafers that had been thinned everywhere to the pinch-off thickness by the anodization process. This caused devices fabricated on ion-implanted wafers to also suffer from low source-to-drain breakdown voltage and high saturation voltage. Ion-implanted wafers have yielded devices with S-parameter characteristics comparable to the better results with epitaxially grown wafers. Devices from ion-implanted wafer A28C, for example, showed a maximum stable gain (MSG) of 12 dB and a 50 ohm to 50 ohm gain (S_{21} gain) of -1.3 dB at 12 GHz.

The available implantation depth (approximately 0.25 μm) did not allow one to create a recessed gate structure to improve the source-to-drain breakdown voltage. Effort was therefore devoted to developing a process to implant n^+ regions selectively in the source and drain regions. Initially a layer of photoresist was employed as an implantation mask. This proved unsatisfactory for two reasons. First, the photoresist was hardened by the implantation conditons, making it very difficult to remove completely. Even when plasma stripping in oxygen was used to remove the photoresist, the surface of the wafer became hazy during the annealing procedure, indicating the presence of some contamination layer. A second problem with this technique was that registration to the implanted source and drain areas was difficult. Alignment marks could be produced by anodization of the wafer in the dark. Since the n layer was thinner than the pinch-off thickness, anodization in the dark

identified the n^+ regions by selectively oxidizing them. The patterns produced in this way had rather diffused edges, making alignment difficult.

In an attempt to cure the photoresist removal problem and simultaneously produce registration marks, selective ion implantation through openings in a Si_3N_4 masking layer was investigated. The first wafer processed by this technique, A62C#1, was prepared in the following sequence. First, the n layer was implanted uniformly across the wafer, but not annealed. Next, a Si_3N_4 masking layer was deposited by the plasma deposition technique. The source and drain regions were then defined in photoresist and plasma etching was used to remove the exposed Si_3N_4 prior to giving the wafer an n^+ ion implant. Prior to annealing, the photoresist was removed by plasma stripping and the Si_3N_4 layer was removed everywhere except at the wafer edges to provide registration marks. After annealing, depositing the ohmic contacts, and sintering, no conduction (<1 μA) was observed between the source and drain. Problems with the ohmic contact metallization were ruled out as the cause of the difficulty because an epitaxial layer wafer metallized and sintered in the same run showed normal contact formation.

The lack of activation of the implanted n layer was surprising because a control sample of the original wafer which was given the n-layer implant, but had not seen the Si_3N_4 deposition or removal process, showed a normal n-layer profile with a peak doping density of $1x10^{17}$ cm^{-3}. The exact nature of the problem with the Si_3N_4 selective implant technique was not determined. However, the Si_3N_4 deposition temperature could have been responsible for a detrimental change to an implanted but unannealed layer.

The ion-implantation sequence has now been modified to avoid exposing unannealed implanted layers to the Si_3N_4 deposition process. However, the effectiveness of this process modification has not yet been fully evaluated.

F. GaAs FET PACKAGING

It is necessary to ensure that FET mounting in a package or circuit is carried out without any added parasitic reactances in order to take full advantage of the intrinsic device capability. This is particularly true when high-performance X-band devices are required. It is also desirable to have a device package or carrier which enables one to characterize the device on a

network analyzer without having to commit it to any specific circuit. We have developed a carrier design which meets these objectives.

One of the parasitic reactances which degrade device performance in common source operation is the parasitic inductance from source to ground. In the device equivalent circuit, such parasitic inductance is equivalent to a resistance at the device input which degrades both available gain and noise figures. For low source-to-ground inductance it is important that the source contacts be as close to the rf ground as possible. We have developed a technique for flip-chip bonding the FET sources to a carrier which forms the rf ground plane. Our experimental results show that flip-chip mounting results in a 2- to 3-dB increase in the maximum available gain (MAG). An additional advantage of flip-chip mounting is that the device thermal resistance is decreased, leading to lowered junction temperature and improved reliability.

The source and drain contacts of our GaAs FETs are on the same level. In order to flip-chip bond the FET pellet, it is necessary to raise the source pad in elevation with respect to the drain pad. This is accomplished by plating up 15-μm-thick posts on the source pads. During this program period, we have developed the technology for plating posts.

Once the source pads are raised in elevation, wires or ribbons are bonded onto the gate and drain pads. For I- and J-band devices, wide, low inductance Au ribbons are used. Gold ribbons are bonded to the gate and drain pads. The pellet is flip-chipped onto the pedestal of a carrier by thermocompression bonding. The flying gate and drain leads are then bonded.

Figure 60 is a photograph of two FETs flip-chipped on the carrier. The carrier consists of a gold-plated OFHC copper base and two ceramic standoffs. The copper base has dimensions of 0.15x0.46x0.064 cm^3 (0.060x0.180x0.025 $in.^3$). The 0.064-cm-thick ceramic standoffs are metallized on both surfaces. Gold straps are bonded from the drain pad of the FET to one standoff and from the gate pad to the other standoff. After the GaAs chip is mounted on the carrier, any subsequent handling and wire bonding are done to the carrier without disturbing the FET. The flip-chip mounting of an FET pellet onto a carrier is easily accomplished by a flip-chip bonder (Kulicke & Soffa*, Model No. 578-2). By the use of a partially transparent prism, the operator can see both the top carrier surface and the FET pattern. Therefore, the FET source pads can be aligned to the carrier bonding surface to within a few-micrometer accuracy.

*Kulicke and Soffa, Inc., Horsham, PA.

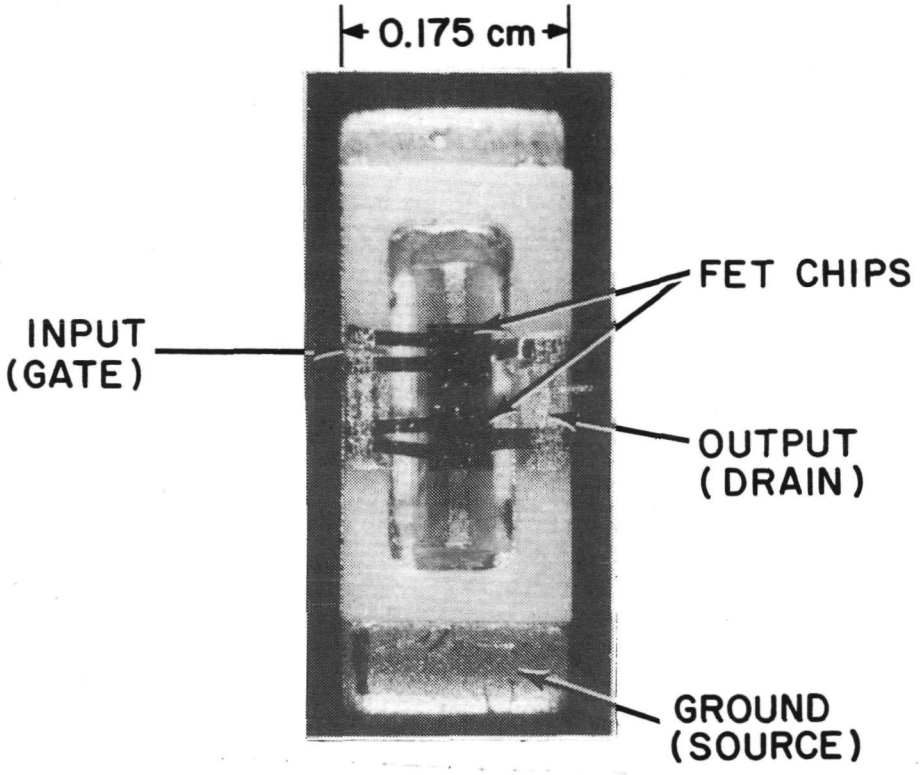


Figure 60. Photograph of two FET pellets flip-chip mounted on a carrier.

Figure 61 is a photograph taken from the flip-chip bonder's microscope. The FET pattern is aligned to the carrier bonding surface ready for flip-chip mounting. The gate and the drain ribbons are also aligned to the bond pads on the standoff.

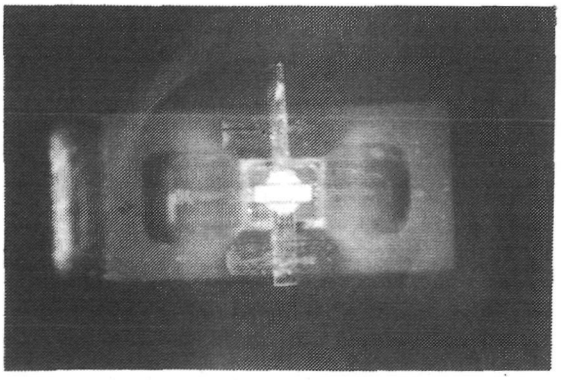


Figure 61. Photograph taken from the flip-chip bonder's microscope. A 16-gate FET is aligned to the carrier ready for flip-chip mounting.

G. THERMAL CONSIDERATIONS

1. Thermal Analysis

One of the most important parameters in the design of a power FET is the maximum temperature rise in the channel. High operating temperature not only degrades the device performance but also greatly reduces the reliability of the device. It is crucial that the device thermal resistance be kept as small as possible. Since the thermal conductivity of GaAs is only 0.3 W/cm-°C while that of copper is 4 W/cm-°C, it is highly desirable to remove the heat through a minimum amount of GaAs. A flip-chip package meets this goal. In a flip-chip mounted device, the thermal flux spreads into copper after only 4 to 6 μm of GaAs. By comparison, in an up-side-mounted device, the thermal flux has to travel through about 100 μm of GaAs before it reaches a copper heat sink. In this section, we will compute the thermal resistance of our proposed 1-W, single-cell device for both up-side and flip-chip mounting.

a. Up-side Mounting - Figure 62 is a schematic diagram showing the thermal flux pattern in an up-side-mounted device. Since GaAs is very fragile, the minimum wafer thickness that can be handled without breakage is about 100 μm. Selective etching of the GaAs substrate down to a few micrometers and refill of this hole with metal is not desirable, since differential thermal expansion of the refilled substrate may cause the GaAs to crack. Therefore, we will assume that the thermal path length in GaAs is 100 μm for the up-side-mounted case.

Referring to Fig. 62, we divide the device thermal resistance into two parts. The first part is the thermal resistance of the 100-μm-thick layer of GaAs (Region I). The second part is the thermal resistance of the copper heat sink (Region II). The Region I configuration is similar to that of a low-mu triode. The thermal resistance in Region I can be obtained by replacing the capacitance of the low-mu triode by thermal conductance, and replacing the permittivity by thermal conductivity. The capacitance of a low-mu triode has been derived by Spangenberg [15]. By making appropriate substitutions, we can show that the Region I thermal resistance is:

$$R_{TH1} = \frac{1}{K_{GaAs}} \left[\frac{d_{gp}}{d} - \frac{1}{\pi} \ell_n \left(2 \sin \frac{0.125\pi \ell_g}{d} \right) \right] \quad \frac{°C\text{-cm gate}}{W} \qquad (33)$$

15. K. R. Spangenberg, Vacuum Tubes (McGraw-Hill Book Co., NY, 1948), pp. 125-130.

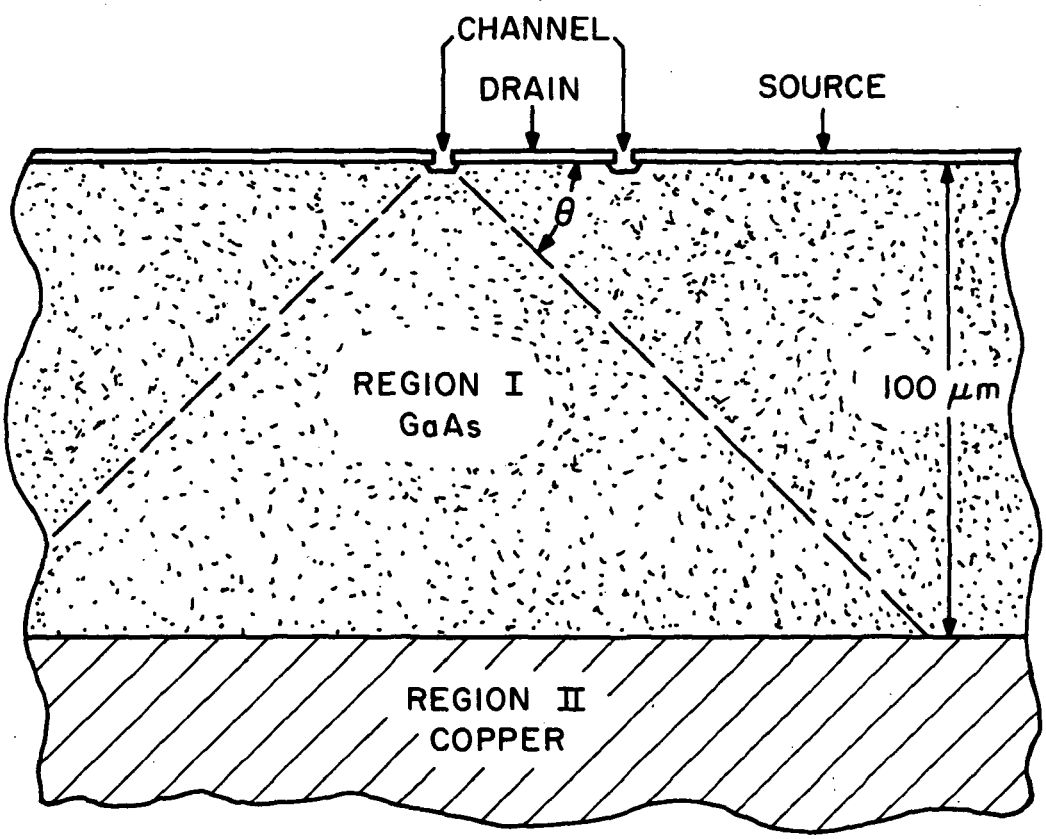


Figure 62. Schematic diagram showing the thermal flux of an up-side mounted GaAs FET.

where K_{GaAs} = 0.3 W/(°C-cm) is the GaAs thermal conductivity, d is the gate center-to-center separation, ℓ_g is the gate length, and d_{gp} = 100 μm is the thickness of the GaAs wafer. In our FET pattern, the gates are not uniformly spaced. They were separated by alternate drain and source contacts. The drain contact is 23 μm long and the source contact is 51 μm long. For simplicity, we will assume a uniform spacing of 38 μm between the gates. Assuming a gate length of 1 μm, we can calculate the thermal resistance in Region I to be:

$$R_{TH1} = 12.88 \frac{°C\text{-cm gate width}}{W} \tag{34}$$

For the 1-W, single-cell pattern, the total gate width is 2400 μm. Thus, the thermal resistance in Region I is

$$R_{TH1} = 53.67\ °C/W \tag{35}$$

The thermal resistance in Region II can be calculated by assuming a uniform heat source on top of the copper heat sink. Assuming a 45° thermal

spread angle in the 100-μm-thick GaAs, the area of the uniform heat source on copper heat sink is 350x636 μm. The thermal resistance of a rectangular heat source of dimensions ℓ x W on a semi-infinite heat sink can be expressed as:

$$R_{TH2} = \frac{1}{2K_{Cu}(\ell-W)} \ell_n \left(\frac{\ell}{W}\right) °C/W \quad (36)$$

In deriving the above expression a thermal spread of 45° is assumed. Using K_{Cu} = 4 W/(°C-cm), ℓ = 658 μm, and W = 350 μm, we obtain

$$R_{TH2} = 1.1°C/W \quad (37)$$

Recall that the thermal resistance in Region I was 53.67°C/W. Thus, as expected, most of the thermal resistance of the device is contributed by the 100-μm-thick GaAs. The total thermal resistance for a up-side-mounted FET is, therefore,

$$R_{TH,up} = \frac{1}{K_{GaAs}} \left[\frac{d_{gp}}{d} - \frac{1}{x} \ell_n \left(2 \sin \frac{0.125\pi\ell_g}{d}\right)\right] + \frac{1}{2K_{Cu}(\ell-W)} \ell_n \left(\frac{\ell}{W}\right) °C/W \quad (38)$$

For a 1-W, up-side-mounted FET, the total thermal resistance is

$$R_{TH,up} = 54.8°C/W \quad (39)$$

This is an optimistic estimate. The actual thermal resistance of the device is expected to be slightly higher.

It can be seen from Eq. (38) that the thermal resistance of an up-side-mounted FET depends strongly on the GaAs thickness. Figure 63 is a plot of calculated thermal resistance of a 16-gate (1-W) FET as a function of GaAs wafer thickness for different gate-to-gate separation. For a small gate-to-gate separation of 5 to 10 μm, the thermal resistance is about 80°C/W for a wafer thickness of 50 μm. Even when the gate-to-gate spacing is in the 30- to 50-μm range, the wafer thickness has to be less than 30 μm to achieve a thermal resistance of 24°C/W to be compatible with the flip-chip case.

b. Flip-Chip Mounting - Figure 64 is a schematic diagram showing the heat flow in a flip-chipped device. Heat is generated in the channel regions of the FET. It travels through only 6 μm of GaAs and reaches the plated source posts. The plated gold source post is 43 by 20 μm high. The drain stripe is 23 μm long. The channel length is approximately 1 μm. We divide the thermal resistance into four parts. Region I is GaAs; Region II is the

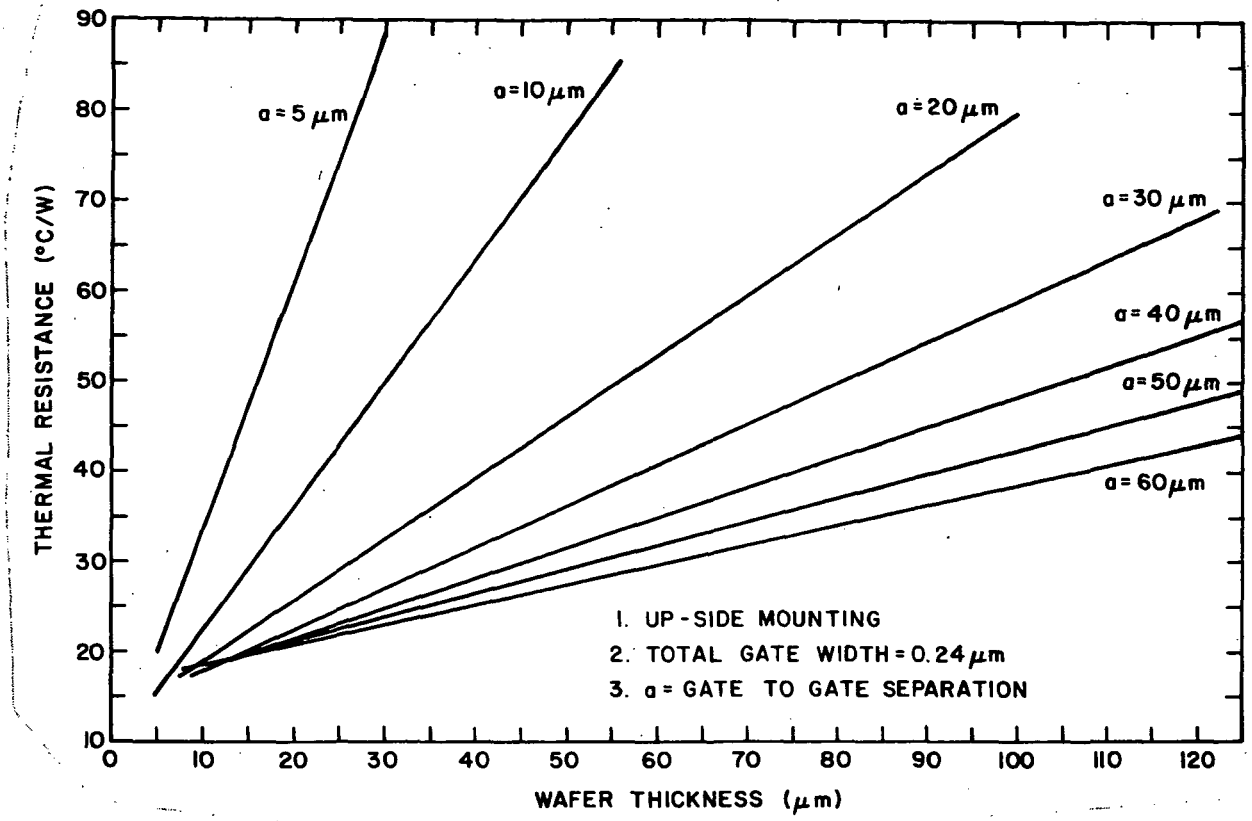


Figure 63. Thermal resistance of a 16-gate FET mounted epi side up. The total gate width is 0.24 cm, designed for 1-W output power.

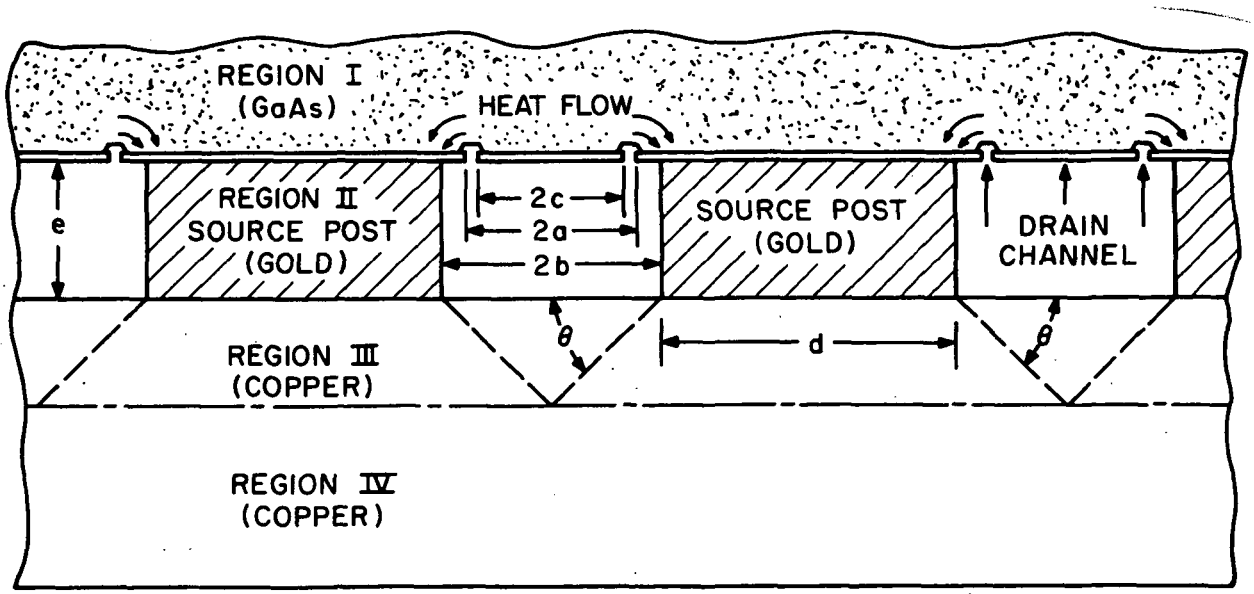


Figure 64. Schematic diagram showing heat flow in flip-chipped GaAs FET. 2a = 25 μm, 2b = 41 μm, 2c = 23 μm, d = 35 μm, e = 20 μm.

source posts; Region III is part of the copper heat sink in which the thermal fluxes generated by each channel do not overlap; and Region IV is the remainder of the copper heat sink in which the thermal fluxes overlap.

In Region I, heat is generated in the channels and then travels through GaAs to the source posts. This configuration is equivalent to a pair of coplanar waveguides. The thermal conductance in Region I can be calculated by replacing the permittivity by the thermal conductivity, and capacitance by thermal conductance.

The capacitance of a coplanar waveguide has been derived by Wen [16]:

$$C = (\varepsilon_r + 1)\, \varepsilon_o \frac{2K(a/b)}{K'(a/b)} \tag{40}$$

where ε is permittivity, $K(k)$ is the complete elliptical integral of the first kind, $K'(k) = K(k')$, and $k' = (1-k^2)^{1/2}$. The dimensions a and b are shown in Fig. 64.

For a drain contact (Fig. 64) between two source posts, there is no heat flow and the contact temperature must be uniform. Therefore, we can treat the drain contact as the center conductor and the two adjacent source posts as ground planes. The thermal resistance in Region I is, therefore,

$$\bar{R}_{TH1} = \frac{1}{K_{GaAs}} \frac{K'(a/b)}{2K(a/b)} \frac{°C\text{-cm drain width}}{W} \tag{41}$$

In the derivation of Eq. (41) from Eq. (40) the coefficient of the elliptic integrals has been reduced to $\varepsilon_r \varepsilon_o$ because there is no heat flow through air. In our case $a/b = 0.61$. Therefore, R_{TH1} can be calculated to be

$$\bar{R}_{TH1} = 1.88 \frac{°C\text{-cm drain width}}{W} \tag{42}$$

Since the total gate width is 2400 μm and there are two gates per drain, the total drain width is 1200 μm. Hence, the thermal resistance in Region I is

$$\bar{R}_{TH1} = 15.68°C/W \tag{43}$$

16. C. P. Wen, "Coplanar-Waveguide Directional Couplers," IEEE Trans. Microwave Theory and Tech. MTT-18, 318 (1970).

Region II consists of 35- by 20-μm-high gold posts. The thermal conductivity of gold is K_{Au} = 3.16 W/(°C-cm). The thermal resistance per unit source width is given by

$$\bar{R}_{TH2} = \frac{e}{K_{Au}d} = \frac{20}{3.16x35} = 0.18 \frac{°C\text{-cm source width}}{W} \tag{44}$$

There are nine source posts, each 150 μm wide. The total source width is thus 1350 μm. Hence, the thermal resistance in Region II is

$$\bar{R}_{TH2} = 1.34°C/W \tag{45}$$

Region III is copper in which the thermal fluxes do not overlap and are thus independent. The contribution of Region III to device thermal resistance is very small. We will use an average length for estimation of R_{TH3}.

$$\bar{R}_{TH3} = \frac{b}{K_{Cu}(b+d)} = 0.12 \frac{°C\text{-cm source width}}{W} \tag{46}$$

So that the thermal resistance in Region III is:

$$\bar{R}_{TH3} = 0.86°C/W \tag{47}$$

Region IV is copper in which the thermal fluxes overlap. We assume a uniform heat source on a semi-infinite heat sink. The heat source is rectangular with a cross section of 636x177.5 μm. The thermal resistance in Region IV is thus given by

$$\bar{R}_{TH4} = \frac{1}{2K_{Cu}(\ell-W)} \ell_n \frac{\ell}{W} = 3.48°C/W \tag{48}$$

Adding Eqs. (43), (45), (47), and (48), we obtain the total thermal resistance for the flip-chip mounted, single-cell, 1-W pattern to be

$$\bar{R}_{TH\ Flip} = 21.05°C/W \tag{49}$$

Recall that the thermal resistance for the same 1-W pattern when up-side mounted is 54.8°C/W [Eq. (39)]. Therefore, the thermal resistance of an up-side-mounted device is more than twice that of a flip-chip-mounted device.

The temperature rise for a typical flip-chip, 1-W FET can be calculated. Assuming a device operating at 25% power-added efficiency with a 1-W output,

3 W are dissipated as heat in the FET. Temperature rise in the device is found from Eq. (42) as

$$\text{Temperature rise} = (21.05°C/W)\ (3\ W)$$
$$= 63.2°C$$

Therefore, the channel temperature of the 1-W FET is about 100°C. Recent reliability studies indicate a MTBF of 10^9 h for a low-noise FET operating at 80°C.

Figure 65 shows the calculated thermal resistance of a 16-gate FET (2400-μm total gate width) as a function of gate-to-gate separation. When the gate-to-gate separation is less than 5 μm, the spreading thermal resistance becomes very large. Figure 66 shows the relative contribution of thermal resistance from the GaAs and the metal for a 16-gate flip-chip FET. Even with 4-μm thermal path in GaAs, the thermal resistance of the GaAs part is still higher than that in the metal. In our FET pattern design, we have chosen the dimension such that the total temperature rise is less than 100°C above ambient to ensure reliable operation.

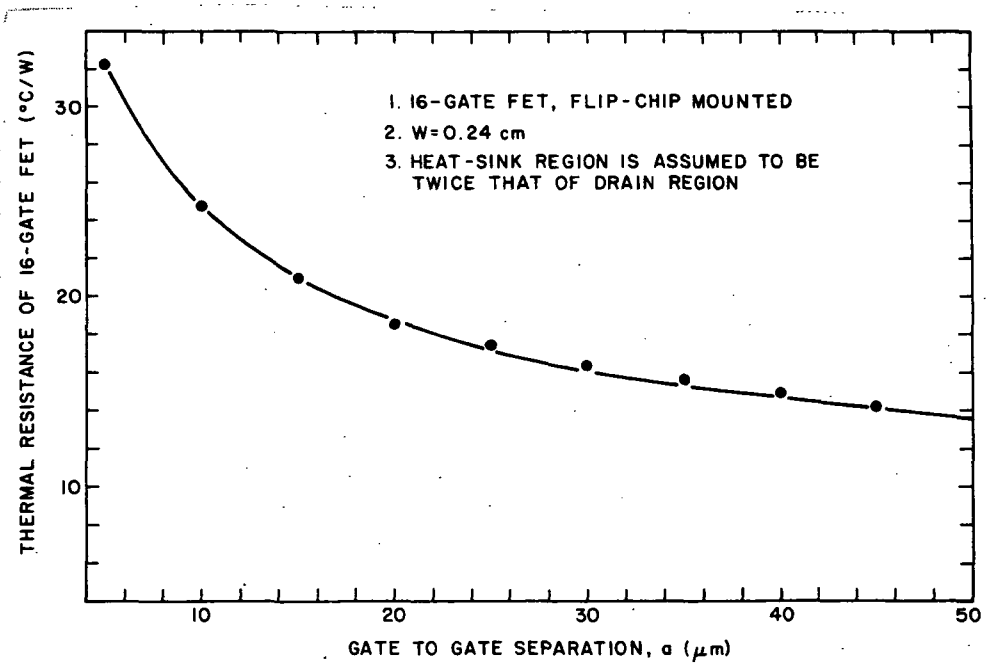


Figure 65. Thermal resistance of a flip-chip-mounted 16-gate GaAs FET as a function of gate-to-gate separation.

In the above discussion, we have chosen the 16-gate (2400-μm) FET as an example. The calculated thermal resistance of various types of flip-chip packaged FETs is summarized in Table 13. The total gate widths range from

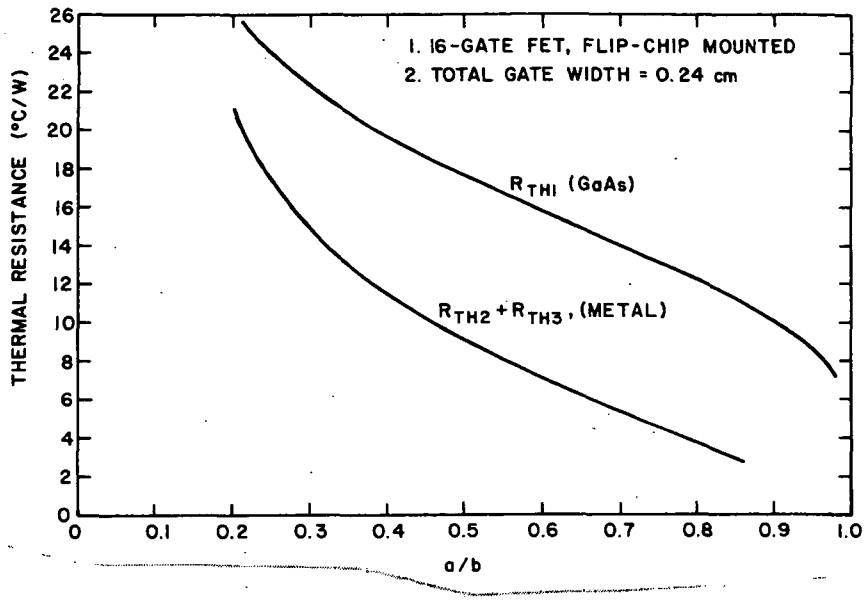


Figure 66. Relative contribution of thermal resistance in GaAs and in heat-sink as a function of heat sink ratio a/b. Calculation is made for 16-gate FET, flip-chip mounted total thermal resistance is the sum of the two curves.

TABLE 13. FET THERMAL RESISTANCE

Designation	2G	4G	8G	16G	32G	48G
Gate Stripes per Cell	2	4	8	16	32	200
Gate Stripe Width (μm)	150	150	150	150	150	200
Gate Width per Cell (μm)	300	600	1200	2400	4800	9600
No. of Cells per Pellet	1	5	1	1	1	1
Drain Contact Width (μm)	25	25	25	12	12	12
Source Post Width (μm)	50	50	50	30	30	30
Design Output Power (μm)	0.15	0.25	0.5	1.0	2.0	4.0
Calculated Flip-Chip Cell Thermal Resistance (°C/W)	168	84	42	21	11	6

300 to 9600 μm and are designed for different power output. The thermal resistance of the FETs is roughly inversely proportional to the total gate width. Thus, the operating temperature is nearly constant regardless of the output power level. The designed operating temperature for all the FETs listed in Table 13 was, in all cases, less than 100°C for a 20°C ambient. We feel that low operating temperature is an important factor to achieving high reliability operation. For satellite communications applications, an operating temperature of less than 110°C is highly desirable.

2. Thermal Resistance Measurements

An infrared scanning microscope (Barnes Engineering* Model RM-24) is used for the measurement of the FET operating temperature and the thermal resistance. A schematic diagram of the IRSM system is shown in Fig. 67. The FET is mounted on a platform, and two precision stepping motors controlled by a computer are used to move the platform in the x and y directions. The mechanical resolution of the stepping motors is 1.6 μm, and the reset error is less than 2 μm. This resettability is important for the calibration of the base temperature. The two stepping motors are driven by two computer-controlled burst-pulse generators. The control unit also contains a temperature controller that powers a heater unit in the platform. To measure the FET operating temperature, a flip-chip bonded FET is mounted on the x-y platform and it is biased at the normal operating condition. The infrared radiation across the FET surface is measured by stepping the platform. Since GaAs is almost transparent to infrared, the infrared microscope "sees" the active region through the GaAs substrate provided that the substrate side is not metallized. To deduce the device temperature from the above measurement, the emissivity is measured by rescanning the device without bias and while heated uniformly at a specified temperature. A computer is used to process the measured data at each stepping point. Finally, the temperature profiles of the FET are automatically plotted.

Figure 68 is the temperature profile along the center of an FET pellet. The peak temperatures correspond to the drain region and valley temperatures correspond to the source region. The peak temperature of 85°C corresponds to a thermal resistance of this 5-cell FET of 19°C/W. Recall that the thermal

*Barnes Engineering, Inc., Stanford, CT.

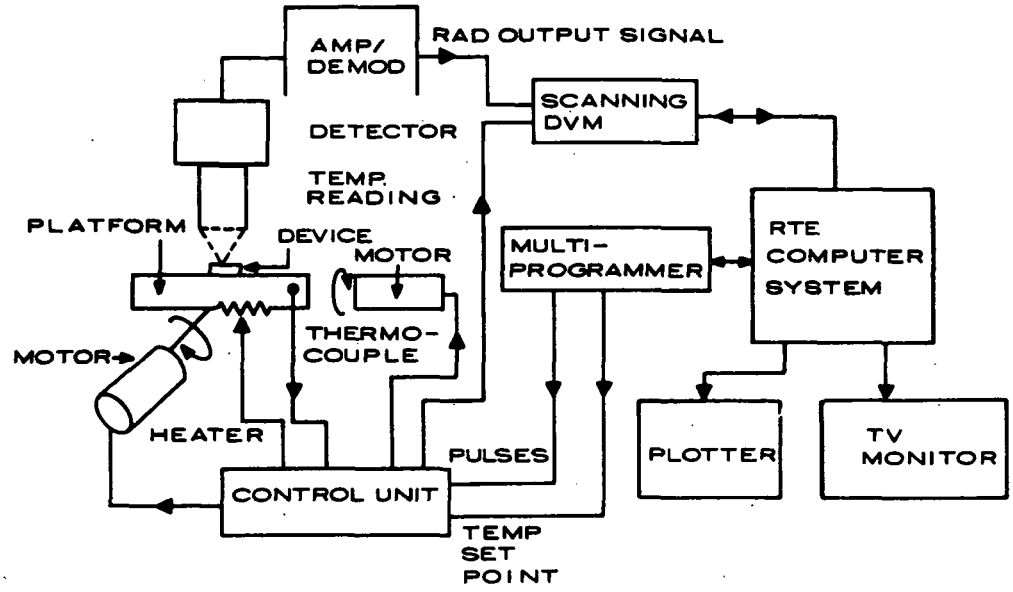


Figure 67. System diagram of computer-controlled infrared microscope.

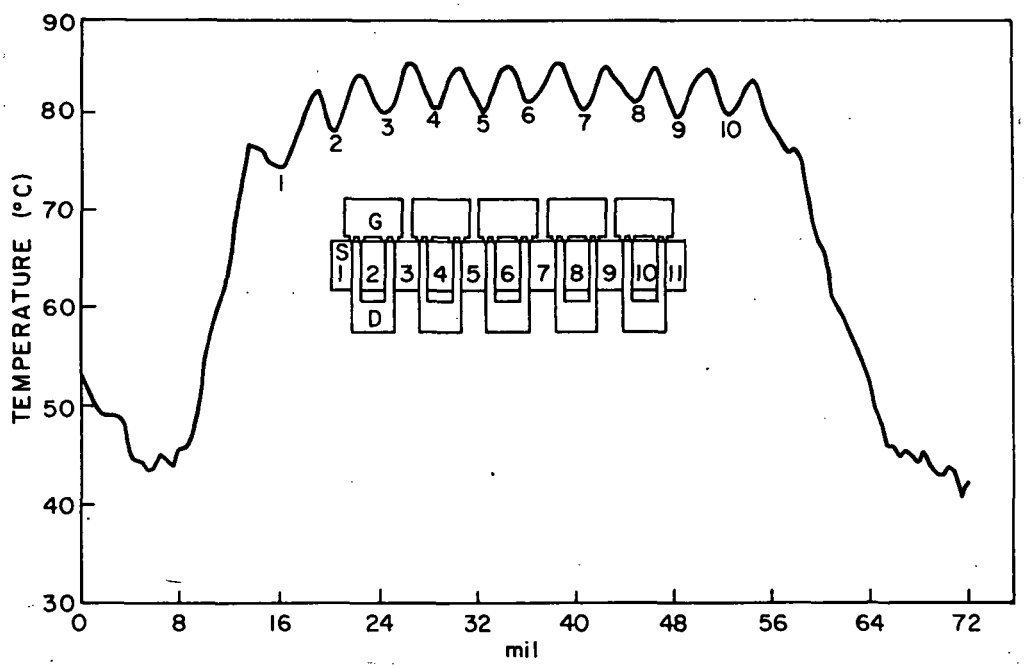


Figure 68. Temperature profile of a 5-cell 4-gate FET.

resistance of a single-cell, 4-gate FET is 80°C/W. With all five cells in parallel, the theoretical thermal resistance is 16°C/W. Figure 69 is an example of a poorly bonded FET; this is a 16-gate, 2400-μm device. It is

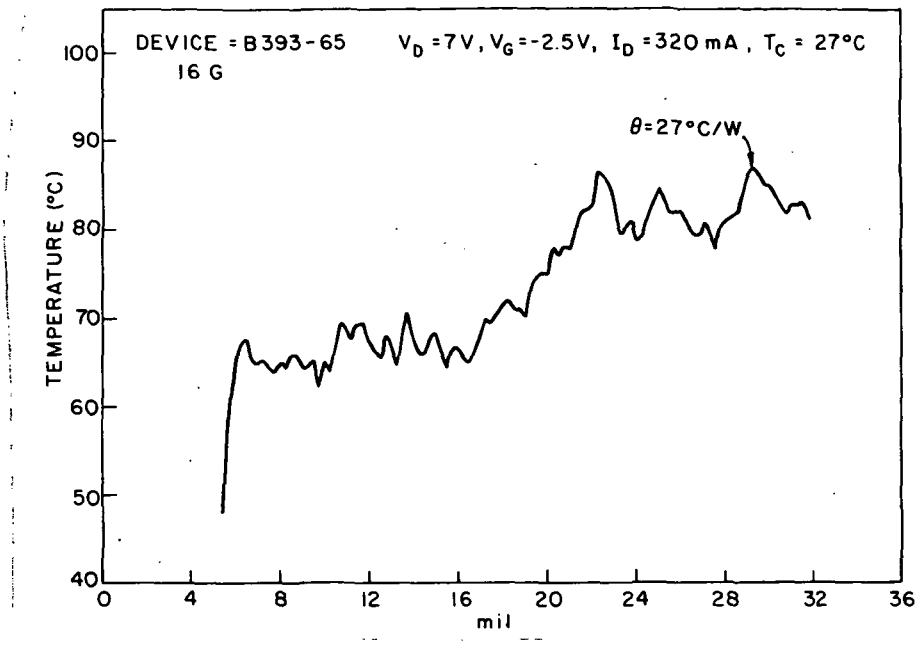


Figure 69. Measured operating temperature of 16-gate FET.

clear that the bond is better at the left-hand side of the chip than that at the right-hand side. The measured thermal resistance is 27°C/W with a peak temperature of 90°C. The calculated thermal resistance is 24°C/W.

H. EQUIVALENT CIRCUIT MODELING AND IMPEDANCE MATCHING FOR HIGH-POWER, HIGH-FREQUENCY DEVICES

One of the problems in the development of high-power, high-frequency FETs is the low FET input and output impedances. Unless impedance matching is provided near the GaAs FET, the losses in the transmission line may be so high that no useful gain and power can be transferred from the device to the outside world. To avoid this problem one can partially match the FET impedances at the chip terminals. To prepare for the partial impedances matching effort, a precise knowledge of the FET input and output impedances (S-parameters) is essential. The S-parameters can be obtained either by network analyzer measurements in the 13- to 15-GHz band, or by deducing the 13- to 15-GHz S-parameters from X-band S-parameters through an equivalent circuit. The advantage of the latter approach is that the X-band S-parameters can be measured more accurately and readily than direct measurement of the Ku-band S-parameters. If the equivalent circuit is reasonably good, this equivalent circuit approach will be more accurate and convenient than the direct measurement.

1. Equivalent Circuit Modeling

We have developed a computer program to calculate the values of the equivalent circuit elements from the S-parameters. Using this program, we can calculate the values of the equivalent circuit elements from the measured low-frequency S-parameters. We then derive the high-frequency S-parameters from this calculated equivalent circuit. In order to evaluate the accuracy of the equivalent circuit and the method of deriving the values of the equivalent circuit elements, we decided to carry out the model at X-band first. Using an 8-gate FET from wafer C221, we measured the S-parameters from 4 to 12 GHz. Using our computer program, we calculated the equivalent circuit from the measured S-parameters as shown in Fig. 70. Note that this equivalent circuit includes both the FET intrinsic impedances and the packaging parasitic impedances. The source parasitic inductance, L_s, has a very low value of 0.01 nH as expected from the flip-chip packaging.

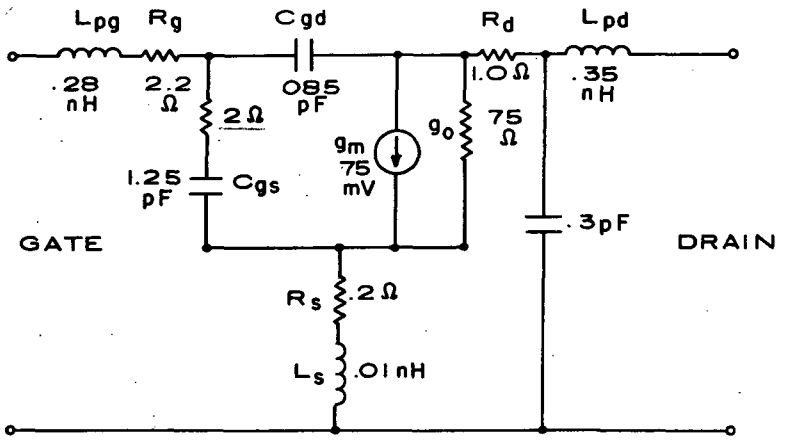


Figure 70. Equivalent circuit derived from measured S-parameters. The FET is an 8-gate continuous gate from wafer C221.

The input capacitance C_{gs} has a relatively large value of 1.25 pF. It resonated with the gate bonding lead inductance (L_g = 0.28 nH) at about 7.6 GHz. Hence, it is important to reduce L_g to improve the input resonant frequency. In our 8-gate FET design, there are two gate bonding pads to accommodate two ribbon bonds from the gate for the reduction of the lead inductance.

Table 14 shows the measured values of S_{11}, S_{21}, S_{12}, and S_{22} from 4 to 12 GHz. Table 15 shows the calculated S-parameters using the equivalent circuit model of Fig. 70. With the help of this model and the computer program, we also calculated the S-parameters of this FET from 12 to 18 GHz. These results are shown in Table 16.

TABLE 14. MEASURED S-PARAMETERS OF AN 8-GATE FET

C221-2 8G CG -1V, 120MA @ 10V DECEMBER 5, 1977

S11 MAG	S11 ANG	S21 MAG	S21 ANG	S12 MAG	S12 ANG	S22 MAG	S22 ANG	FREQ MHZ
.841	-140.8	1.937	71.4	.071	7.4	.320	-109.7	4000.0
.820	-145.4	1.851	67.2	.070	4.7	.343	-114.2	4200.0
.816	-148.9	1.780	64.6	.069	4.3	.344	-115.4	4400.0
.814	-153.5	1.708	60.6	.068	1.3	.357	-118.4	4600.0
.828	-155.8	1.673	58.7	.067	2.8	.367	-118.7	4800.0
.837	-160.2	1.625	54.9	.075	-2.7	.377	-122.5	5000.0
.842	-163.7	1.577	51.6	.071	-5.6	.379	-123.0	5200.0
.834	-168.2	1.509	47.1	.070	-8.8	.386	-124.9	5400.0
.839	-170.9	1.456	44.2	.070	-11.2	.382	-126.5	5600.0
.851	-172.8	1.410	40.6	.068	-13.9	.388	-128.0	5800.0
.865	-176.6	1.365	37.2	.067	-16.1	.387	-130.0	6000.0
.861	-178.7	1.311	34.5	.066	-18.6	.387	-131.4	6200.0
.855	177.7	1.263	30.7	.064	-22.1	.386	-133.6	6400.0
.844	174.7	1.190	28.0	.064	-24.5	.392	-135.8	6600.0
.842	172.9	1.143	25.1	.063	-26.5	.390	-138.1	6800.0
.847	171.5	1.104	22.5	.064	-28.1	.394	-140.5	7000.0
.837	169.4	1.062	19.1	.063	-31.2	.404	-144.1	7200.0
.819	167.9	1.041	15.7	.064	-33.7	.410	-146.9	7400.0
.810	166.5	1.000	13.7	.064	-35.3	.430	-150.1	7600.0
.809	166.3	.973	12.0	.066	-36.9	.450	-153.6	7800.0
.819	164.4	.945	9.6	.067	-39.1	.471	-156.6	8000.0
.813	164.0	.871	6.9	.063	-46.9	.483	-162.7	8200.0
.832	164.5	.869	6.5	.061	-44.4	.491	-164.0	8400.0
.828	161.4	.849	2.2	.061	-46.8	.518	-167.0	8600.0
.803	159.3	.808	-1.1	.061	-48.9	.521	-167.5	8800.0
.815	159.9	.790	-2.2	.061	-46.4	.550	-168.5	9000.0
.819	159.4	.770	-5.1	.064	-47.2	.561	-167.6	9200.0
.804	159.6	.741	-7.6	.068	-49.1	.582	-168.2	9400.0
.804	160.1	.711	-7.8	.068	-53.7	.584	-167.8	9600.0
.801	158.0	.704	-9.3	.066	-54.7	.603	-166.3	9800.0
.803	157.5	.701	-10.7	.067	-54.1	.608	-163.7	10000.0
.817	155.8	.707	-11.5	.073	-53.7	.644	-163.8	10200.0
.837	153.9	.719	-15.1	.078	-60.6	.642	-163.2	10400.0
.829	152.0	.721	-17.1	.077	-62.2	.634	-162.3	10600.0
.809	148.6	.726	-20.5	.077	-64.5	.633	-161.5	10800.0
.785	144.2	.739	-24.7	.080	-67.3	.632	-163.2	11000.0
.788	141.5	.742	-27.1	.082	-68.4	.612	-162.1	11200.0
.784	137.2	.748	-31.2	.084	-71.1	.596	-163.0	11400.0
.798	133.8	.769	-35.2	.088	-74.7	.586	-166.5	11600.0
.750	130.8	.749	-40.6	.086	-78.4	.543	-171.7	11800.0
.750	127.6	.740	-44.0	.087	-80.9	.500	-174.3	12000.0
.730	124.0	.730	-48.9	.088	-84.5	.475	177.4	12200.0
.721	119.2	.730	-54.2	.089	-88.1	.444	168.2	12400.0

REFL PLANES: 2.10 3.30 TRAN LINE 7.40

Comparing the S-parameter measured in X-band with the S-parameters calculated from the equivalent circuit model, we see that the major discrepancy

TABLE 15. CALCULATED S-PARAMETERS FOR THE SAME FET AS SHOWN IN TABLE 14 USING EQUIVALENT CIRCUIT IN FIG. 70.

TITLE:

FREQ	S11		S21		S12		S22	
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
4000.0	.853	-139.	2.019	87.89	.059	5.647	.231	-106.
4400.0	.848	-145.	1.862	82.82	.060	1.437	.241	-112.
4800.0	.844	-151.	1.723	78.03	.061	-2.48	.252	-117.
5200.0	.841	-156.	1.601	73.50	.061	-6.16	.264	-122.
5600.0	.839	-161.	1.492	69.16	.061	-9.65	.277	-126.
6000.0	.837	-165.	1.395	64.99	.061	-13.0	.290	-131.
6400.0	.836	-169.	1.308	60.96	.061	-16.2	.304	-135.
6800.0	.835	-173.	1.229	57.06	.061	-19.2	.319	-139.
7200.0	.835	-177.	1.157	53.25	.061	-22.2	.334	-143.
7600.0	.835	179.6	1.091	49.54	.060	-25.1	.349	-147.
8000.0	.835	176.4	1.031	45.91	.060	-27.9	.365	-151.
8400.0	.835	173.3	.975	42.35	.059	-30.6	.381	-154.
8800.0	.835	170.3	.924	38.85	.059	-33.2	.397	-158.
9200.0	.836	167.5	.876	35.41	.058	-35.8	.413	-162.
9600.0	.837	164.8	.832	32.02	.058	-38.4	.430	-165.
10000.	.838	162.2	.790	28.69	.057	-40.9	.447	-168.
10400.	.839	159.7	.751	25.41	.056	-43.3	.464	-172.
10800.	.840	157.3	.715	22.17	.055	-45.7	.480	-175.
11200.	.841	154.9	.681	18.98	.054	-48.1	.497	-178.
11600.	.842	152.6	.648	15.83	.054	-50.4	.514	178.4
12000.	.844	150.4	.618	12.72	.053	-52.7	.531	175.3

TABLE 16. CALCULATED S-PARAMETERS AT Ku-BAND FROM EQUIVALENT CIRCUIT IN FIG. 70.

FREQ	S11		S21		S12		S22	
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
12000.	.844	150.4	.618	12.72	.053	-52.7	.531	175.3
12500.	.846	147.8	.582	8.906	.052	-55.5	.551	171.5
13000.	.847	145.2	.549	5.157	.050	-58.2	.572	167.8
13500.	.849	142.7	.517	1.475	.049	-60.8	.592	164.1
14000.	.851	140.3	.488	-2.14	.048	-63.4	.611	160.6
14500.	.854	138.0	.460	-5.68	.047	-65.9	.630	157.1
15000.	.856	135.7	.435	-9.15	.045	-68.3	.649	153.7
15500.	.858	133.5	.410	-12.5	.044	-70.6	.667	150.4
16000.	.860	131.4	.387	-15.9	.043	-72.9	.684	147.2
16500.	.862	129.3	.366	-19.1	.042	-75.1	.701	144.1
17000.	.865	127.3	.346	-22.3	.040	-77.3	.717	141.1
17500.	.867	125.3	.326	-25.4	.039	-79.3	.732	138.1
18000.	.869	123.4	.308	-28.4	.038	-81.3	.747	135.2

is that the S_{21} phase does not fall as rapidly in the calculated values as in the measured values.

2. Impedance Matching for High-Power, High-Frequency Device

One of the important problems to achieving high output power at high frequency is to match the low device impedance to the 50-ohm source impedance. A large impedance mismatch causes excessive loss in the impedance matching network. In addition, if the impedance matching network is more than one wavelength away from the active region, a substantial portion of the available microwave power is dissipated in the resistive component of the inactive zone which is between the impedance matching network and the active region. Consequently, both the microwave output power and the power gain are greatly reduced from the intrinsic device capability. It is well known that a standing wave pattern exists if there is an impedance mismatch. Figure 71 illustrates the concept of the standing wave pattern for the case where the impedance matching network is one wavelength away from the device. For simplicity of illustration, we have assumed that the input and output impedance of the FET are both real and much less than 50 ohm. The high rf current generated in the transmission lines Z_1 and Z_2 of the inactive zones will cause a substantial loss in rf power because of the finite resistance in the transmission lines. For high-power, high-frequency FETs, the losses in the input and output impedance matching networks and in Z_1 and Z_2 of an improperly designed FET can be so high as to render the apparent performance much lower than the FETs intrinsic performance.

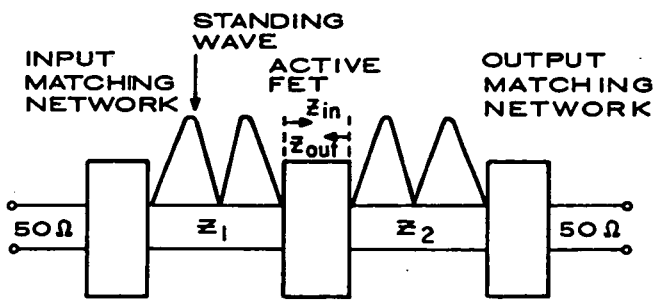


Figure 71. Schematic diagram illustrating the concept of standing wave pattern between the active FET and the impedance matching networks. The losses in the input and output matching networks and in the transmission lines Z_1 and Z_2 can be very large for high-power, high-frequency FETs.

Having recognized the problem, we have devised a solution to achieving the best possible FET performance at high frequency by minimizing the losses in the impedance matching networks and the inactive zones. In order to minimize the loss in the matching network, we limit the impedance mismatch by limiting the total active area per unit cell. If the output power requirement is more than is available from a unit cell, the impedance of each unit cell is matched or partially matched before they are combined.

In order to minimize the loss in the inactive zones, we place the matching networks immediately adjacent to the FET active area; thus, we eliminate the inactive zone. To implement this concept, we design the device pattern to have the metallization lines connecting to the gates and the drains as the first element of the matching network. The microwave power is generated in the channel in the source-gate-drain region. At high frequency the input impedance to the intrinsic FET is largely capacitive which results from the gate-to-source capacitance. Therefore, the metallization line connecting the gate should be inductive. The designed values of this inductance, as governed by the length and width of the lines, are determined by the operating frequency and the gate-source capacitance. In order to provide a bonding area to connect the FET to the outside world, it is often necessary to have a gate pad, drain pad, and/or source pad to facilitate bonding. Therefore, in the FET design we design the size of the bonding pads to achieve a capacitive impedance. As shown in Fig. 72 this gate-source capacitance, metallization line inductance, and gate pad capacitance form a low pass filter to transform the impedance of the intrinsic FET to 50 ohm or close to 50 ohm. Figure 72 (b) shows the conceptual design. The metallization line and the gate are designed to be inductive (L_{gM}) while the gate pad and the gate-source capacitance are capacitive. This C-L-C low pass filter matching network is shown schematically in Fig. 72(b). Similar designs can also be applied to the drain side (output). In this design, the inactive zone is eliminated. In Fig. 72 we show only one source-gate-drain (channel) for simplicity. To achieve high output power, we parallel many channels. Figure 73 shows the input equivalent circuit of a FET with only one gate channel [Fig. 73(a)] and a FET with n-gate channels in parallel [Fig. 73(b)]. We let R_g be the gate metallization resistance. The rf voltage across the gate capacitance, C_{gs}, modulates the FET channel to

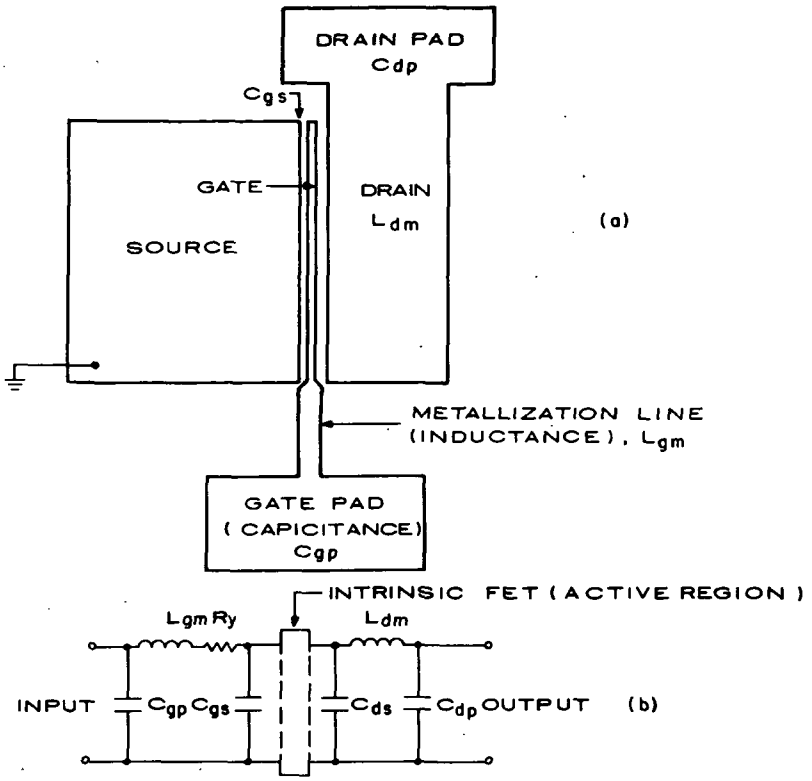


Figure 72. Schematic diagram illustrating the design concept. The impedance matching is adjacent to the active region, thus eliminating the inactive zone.

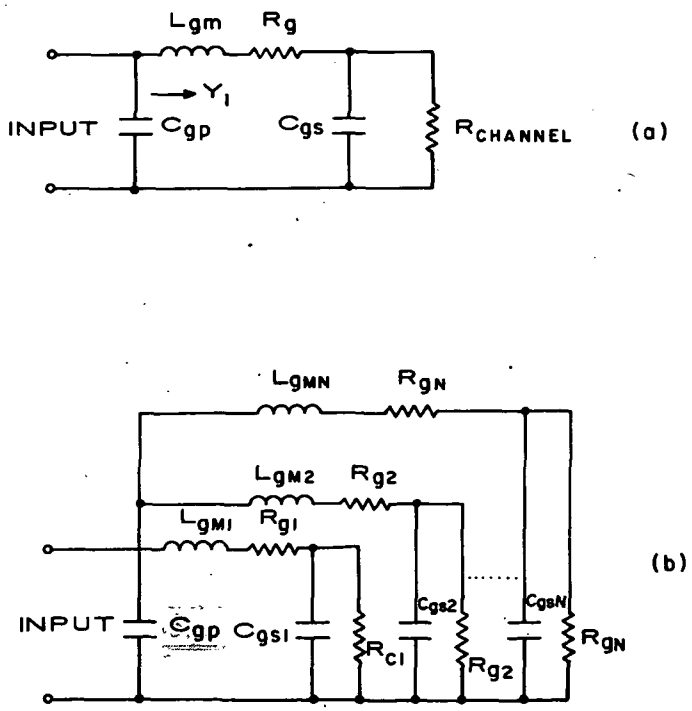


Figure 73. Input equivalent circuit of (a) single-channel FET and (b) n-channel FET.

control the current flow. If we let Y_1 be the input admittance of a single-channel FET excluding the gate pad capacitance C_{gp} [Fig. 73(a)], Y_1 can be expressed as:

$$Y_1 = \frac{1}{R_{g1}+L_{gM1}+[1/R_{CH}+jWC_{gs1}]-1} \tag{50}$$

For a FET with n channels in parallel, the input admittance is:

$$Y_{in} = jWC_{gp} + nY_1 \tag{51}$$

The gate pad capacitance, C_{gp}, is nearly constant in the discrete FETs because there is a minimum size of the gate bonding pad which is about 3x3 mil. The size of the gate pad and hence the value of C_{gp} is designed as a part of the matching network as shown in Fig. 72(b). From Eq. (51), the input impedance of a FET decreases nearly inversely proportionally to the number of channels and to the operating frequency as shown in Eq. (51). In the case of a conventional discrete FET there is usually some inductance and resistance, introduced by the bond wire and the package, in series with Y_{in}. Therefore, a substantial portion of the rf voltage is dissipated across the series inductance and resistance. This voltage drop across the parasitic impedance is especially severe for the case of high-frequency (above 15 GHz) and high-power (above 2 W) FETs. In the next section we will describe a design example in which the parasitic loss is minimized by eliminating the inactive zone and by matching to several low-power FET cells before power combination. This approach has three major advantages:

(1) The loss in the parasitic impedances can be eliminated because there is no unwanted parasitic impedance.

(2) The bandwidth of the FET can be greatly improved because the impedance matching starts right at the terminal of the active channel. There is no unwanted electrical length between the active channel and the impedance matching networks.

(3) The loss in the matching networks is minimized because we match to the low power unit cells (which have high impedance) before combining them.

3. A Numerical Example for the Design of a 3-Cell, 3.5-W J-Band FET

In this section, we present results from a computer simulation for the design of a 3-cell, 3.5-W J-band FET. In doing so, we first show that a large 56-gate single-cell FET is not an acceptable design because the FET's input impedance is too low. We then present a 3-cell FET design for 3.5-W output power.

a. A Single-Cell FET

From our large-signal analysis, we calculated that a total gate width of about 7 mm is required for 3.5-W output power. We will calculate the gain and the input-output impedance (S-parameters) of this single-cell FET by scaling from an existing 1.2-mm FET RCA has developed.

Tables 17 and 18 show the measured small-signal S-parameters and computed small-signal gain of an RCA 1.2-mm power FET. Note that a small-signal gain of about 7 dB can be achieved at 15 GHz. Such a device can generate an output power of about 0.75 W with 4-dB power gain at 15 GHz.

The equivalent circuit of this FET derived from the parameters shown in Tables 17 and 18 is shown in Fig. 74. This equivalent circuit includes the effects of parasitics. Note the very low value of 0.01 nH for the source inductance, a consequence of flip-chip mounting. This equivalent circuit can be used for scaling studies. Table 19 shows the S-parameters of this equivalent circuit. These are in fair agreement with the measured values shown in Table 17. There is some disagreement in the phase angles. This, however, does not affect our discussion of scaling.

We will consider now the scaling of this FET to a size capable of generating 3.5 W at J-band. The resistances R_{gs} and R_{dg} are composed of a parasitic component and a component resulting from the source-gate and gate-drain spacing. Since our FET is symmetrical with source-gate and gate-drain spacings of 0.4 μm, we can estimate the value of the parasitic and intrinsic components. We assume a channel mobility of 3000 $cm^2V^{-1}s^{-1}$ and that the gate is biased at half the pinch-off voltage corresponding to a effective nT of 1.5×10^{12} cm^{-2}. The intrinsic component is then equal to 0.5 ohm. The parasitic components of R_{gs} and R_{dg} can thus be estimated as 1.1 ohm and 0.5 ohm, respectively.

TABLE 17. MEASURED S-PARAMETERS OF FET C182B-89

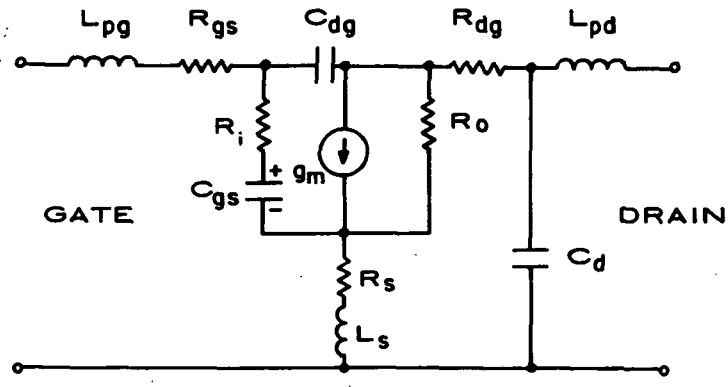
.00 VOLTS, .00 MA (MEAS 1) C182B-89 RG 8 -2 340

FREQ	S11		S21		S12		S22	
(MHZ)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
10000.00	.862	-166	.851	19	.056	-21	.667	-135
10100.00	.874	-166	.894	18	.058	-22	.656	-136
10200.00	.875	-166	.888	15	.058	-23	.656	-137
10300.00	.855	-166	.844	14	.056	-23	.652	-138
10400.00	.855	-166	.848	16	.056	-22	.653	-138
10500.00	.876	-166	.895	15	.060	-22	.668	-138
10600.00	.863	-167	.893	11	.060	-26	.666	-140
10700.00	.856	-167	.857	10	.057	-27	.663	-140
10800.00	.859	-167	.835	9	.055	-28	.667	-140
10900.00	.862	-167	.820	8	.054	-28	.674	-140
11000.00	.862	-168	.798	8	.053	-27	.681	-140
11100.00	.865	-167	.797	9	.052	-26	.686	-139
11200.00	.861	-168	.804	8	.053	-26	.692	-140
11300.00	.866	-168	.800	7	.053	-27	.698	-140
11400.00	.858	-169	.782	6	.052	-28	.700	-140
11500.00	.861	-169	.789	6	.051	-27	.702	-139
11600.00	.847	-169	.770	5	.050	-27	.710	-139
11700.00	.866	-169	.766	5	.050	-26	.731	-139
11800.00	.866	-170	.767	4	.050	-26	.728	-140
11900.00	.873	-170	.776	4	.049	-26	.724	-140
12000.00	.871	-171	.766	3	.049	-26	.714	-140
12100.00	.863	-170	.749	2	.047	-26	.701	-139
12200.00	.874	-170	.757	3	.047	-24	.705	-139
12300.00	.871	-171	.757	2	.047	-23	.699	-138
12400.00	.874	-172	.764	1	.047	-21	.699	-138
12500.00	.882	-172	.776	-0	.049	-20	.701	-138
12600.00	.878	-173	.768	-1	.049	-19	.704	-138
12700.00	.880	-173	.761	-2	.051	-19	.703	-138
12800.00	.885	-173	.750	-2	.052	-20	.704	-139
12900.00	.883	-174	.765	-1	.053	-19	.702	-139
13000.00	.872	-174	.788	-2	.055	-20	.704	-139
13100.00	.877	-174	.780	-3	.055	-21	.718	-140
13200.00	.876	-175	.815	-4	.057	-21	.715	-141
13300.00	.880	-175	.839	-7	.059	-24	.717	-142
13400.00	.876	-176	.827	-9	.058	-27	.721	-143
13500.00	.873	-176	.830	-11	.058	-28	.718	-144
13600.00	.878	-176	.835	-14	.057	-31	.721	-144
13700.00	.869	-177	.793	-18	.054	-33	.728	-145
13800.00	.868	-177	.758	-18	.051	-33	.736	-146
13900.00	.871	-177	.754	-17	.051	-31	.740	-146
14000.00	.874	-177	.739	-17	.049	-30	.743	-147
14100.00	.876	-177	.736	-17	.049	-28	.744	-147
14200.00	.876	-178	.746	-17	.050	-28	.746	-148
14300.00	.877	-179	.770	-17	.051	-27	.746	-149
14400.00	.879	-179	.805	-18	.053	-27	.747	-149
14500.00	.877	-179	.838	-21	.054	-29	.746	-150
14600.00	.884	180	.850	-26	.055	-31	.747	-150
14700.00	.881	179	.844	-30	.055	-33	.743	-151
14800.00	.869	179	.812	-34	.054	-34	.736	-151
14900.00	.872	178	.766	-38	.052	-36	.739	-152
15000.00	.876	178	.724	-39	.051	-36	.741	-152

TABLE 18. SMALL-SIGNAL GAIN CORRESPONDING TO S-PARAMETERS IN TABLE 17

.00 VOLTS, .00 MA (MEAS 1) C182B-89 RG 8 -2 340

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
10000.00	8.89	7.06	-1.40	-24.99	1.23	.19
10100.00	10.47	7.75	-.97	-24.77	1.05	.22
10200.00	10.07	7.70	-1.03	-24.75	1.09	.22
10300.00	7.92	6.63	-1.47	-25.00	1.42	.17
10400.00	8.13	6.69	-1.43	-24.97	1.37	.17
10500.00		7.94	-.96	-24.45	.96	.24
10600.00	9.45	7.50	-.98	-24.49	1.14	.22
10700.00	8.12	6.90	-1.34	-24.87	1.37	.19
10800.00	7.87	6.80	-1.56	-25.13	1.43	.18
10900.00	7.93	6.82	-1.72	-25.38	1.43	.18
11000.00	7.74	6.65	-1.96	-25.56	1.47	.18
11100.00	7.94	6.78	-1.97	-25.60	1.43	.19
11200.00	8.05	6.80	-1.90	-25.52	1.40	.19
11300.00	8.20	6.97	-1.94	-25.57	1.35	.20
11400.00	7.59	6.57	-2.13	-25.74	1.51	.18
11500.00	7.83	6.77	-2.06	-25.86	1.47	.19
11600.00	7.07	6.26	-2.27	-26.05	1.68	.16
11700.00	8.33	7.04	-2.32	-26.01	1.35	.21
11800.00	8.30	7.02	-2.30	-26.06	1.36	.21
11900.00	8.72	7.26	-2.20	-26.13	1.29	.21
12000.00	8.14	6.96	-2.31	-26.23	1.41	.20
12100.00	7.16	6.35	-2.51	-26.51	1.69	.16
12200.00	7.91	6.83	-2.41	-26.50	1.49	.19
12300.00	7.61	6.65	-2.42	-26.62	1.58	.17
12400.00	7.96	6.84	-2.34	-26.50	1.48	.18
12500.00	8.70	7.26	-2.21	-26.28	1.31	.21
12600.00	8.49	7.09	-2.29	-26.12	1.33	.20
12700.00	8.55	7.04	-2.37	-25.83	1.28	.21
12800.00	8.81	7.13	-2.50	-25.76	1.22	.22
12900.00	9.20	7.20	-2.33	-25.55	1.16	.22
13000.00	8.96	7.13	-2.07	-25.21	1.19	.22
13100.00	9.62	7.45	-2.06	-25.17	1.10	.24
13200.00	10.59	7.65	-1.78	-24.84	1.02	.26
13300.00		8.09	-1.53	-24.62	.96	.28
13400.00	10.14	7.87	-1.65	-24.79	1.06	.27
13500.00	9.56	7.78	-1.61	-24.78	1.11	.26
13600.00	9.45	8.02	-1.56	-24.92	1.13	.27
13700.00	8.88	7.36	-2.02	-25.40	1.37	.23
13800.00	7.71	7.06	-2.41	-25.77	1.45	.22
13900.00	7.97	7.17	-2.45	-25.92	1.40	.23
14000.00	8.04	7.14	-2.63	-26.14	1.39	.22
14100.00	8.24	7.19	-2.67	-26.18	1.35	.23
14200.00	8.58	7.31	-2.55	-26.05	1.28	.23
14300.00	9.35	7.63	-2.27	-25.79	1.16	.25
14400.00	10.37	8.10	-1.89	-25.56	1.06	.28
14500.00	10.66	8.37	-1.54	-25.30	1.04	.29
14600.00		8.81	-1.33	-25.16	1.00	.32
14700.00	9.74	8.53	-1.40	-25.24	1.12	.30
14800.00	8.15	7.70	-1.80	-25.41	1.37	.25
14900.00	7.52	7.34	-2.32	-25.66	1.49	.24
15000.00	7.10	6.98	-2.80	-25.84	1.56	.23



L_{pg} = 0.25 nH	R_{gs} = 1.6 Ω	C_{dg} = 0.06 pF
R_i = 1.8 Ω	C_{gs} = 0.9 pF	g_m = 95 mS
R_o = 75 Ω	R_{dg} = 1.0 Ω	L_{pd} = 0.1 nH
R_s = 0.2 Ω	L_s = 0.01 nH	C_d = 0.5 pF

Figure 74. Equivalent circuit of an RCA 1200-μm gate width (8-gate) FET.

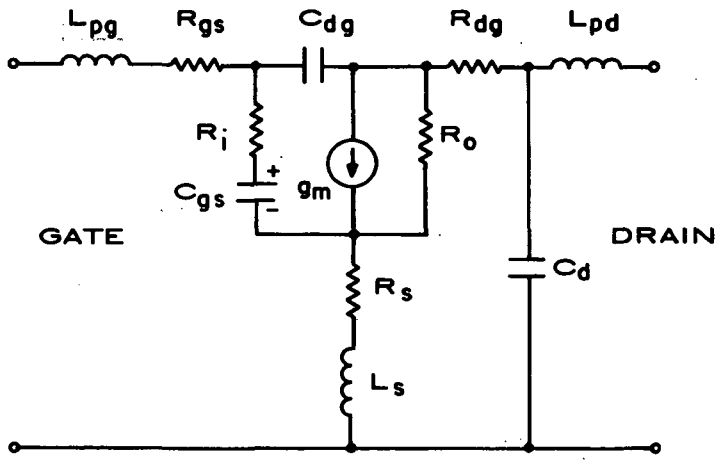
TABLE 19. CALCULATED S-PARAMETERS OF AN RCA 1200-μm-WIDE FET USING FIG. 74

DATA FILE: JG1

FREQ	S11		S21		S12		S22		STAB	
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	K	CMAX
12000.	.848	163.8	.870	25.61	.042	-45.6	.723	-152.	1.027	9.730
12500.	.850	160.9	.816	22.61	.041	-47.3	.735	-154.	1.082	9.301
13000.	.853	158.1	.767	19.71	.040	-49.9	.748	-156.	1.436	8.901
13500.	.855	155.4	.721	16.89	.039	-51.9	.759	-158.	1.490	8.524
14000.	.857	152.8	.679	14.15	.038	-53.8	.770	-160.	1.545	8.168
14500.	.860	150.3	.640	11.50	.037	-55.7	.781	-161.	1.599	7.831
15000.	.862	147.9	.604	8.917	.036	-57.4	.790	-163.	1.653	7.510
15500.	.864	145.5	.570	6.407	.035	-59.1	.800	-165.	1.706	7.204
16000.	.867	143.2	.539	3.965	.034	-60.8	.808	-166.	1.760	6.910

We will now scale-up to an output power of 3.5 W. Clearly, an FET with about seven times the active area of our 1.2-mm (8-gate) FET will be required.

We will scale only the FET intrinsic components and leave the parasitics unchanged. The parasitic mounting impedances are R_{gs} = 1.1 Ω, R_{ds} = 0.5 Ω, and R_s, and L_s. Figure 75 shows the equivalent circuit of the scaled-up FET (56-gate FET). Table 20 shows the computed S-parameters and the small-signal gain of this FET. The maximum available gain GMAX is now reduced to 6 dB from the 7-dB value of the 8-gate FET. More importantly, the input and output impedances of the 56-gate FET are very low (about 2.5 ohm real part) which implies that GMAX is composed mainly of mismatch gain which will be very difficult to realize in practice. It is almost impossible to match this FET over any reasonable bandwidth without paying an excessive gain penalty. We therefore conclude that a large single-cell, 56-gate FET is completely unsuitable for this application.



L_{pg} = 0.25 nH	R_{gs} = 1.17 Ω	C_{dg} = 0.42 pF
R_i = 0.26 Ω	C_{gs} = 6.3 pF	g_m = 665 mS
R_o = 525 Ω	R_{dg} = 0.57 Ω	L_{pd} = 0.1 nH
R_s = 0.2 Ω	L_s = 0.01 nH	C_d = 3.5 pF

Figure 75. Equivalent circuit of an FET with 7 times the active area of that shown in Fig. 74.

TABLE 20. CALCULATED S-PARAMETERS AND GAIN OF A SINGLE-CELL, 56-GATE FET

TITLE:
DATA FILE: JG1

FREQ	S11		S21		S12		S22		STAB	
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	K	GMAX
12000.	.939	140.9	.162	-18.5	.063	-86.3	.989	170.3	2.197	8.693
12500.	.941	139.2	.149	-20.2	.063	-86.3	.982	169.3	2.369	8.316
13000.	.942	137.4	.137	-21.9	.064	-87.2	.983	168.3	2.554	7.959
13500.	.943	135.7	.127	-23.6	.064	-87.7	.984	167.3	2.756	7.620
14000.	.944	134.0	.118	-25.1	.064	-87.9	.985	166.4	2.976	7.297
14500.	.945	132.3	.110	-26.7	.064	-88.0	.986	165.5	3.214	6.989
15000.	.946	130.6	.102	-28.1	.063	-87.6	.987	164.6	3.471	6.696
15500.	.947	129.0	.095	-29.6	.063	-88.9	.988	163.7	3.753	6.411
16000.	.948	127.4	.089	-31.0	.063	-78.6	.989	162.8	4.055	6.140

b. A 3-Cell, 3.5-W J-Band FET

We will now describe the design of a 3-cell FET on an internally matched carrier for 3.5-W output power in J-band. Preliminary calculations based on computer-aided design and simulation will be presented.

The basic building block is an 18-gate, 3.15-mm-gate-width FET for over 1-W output power in J-band. Figure 76 shows a drawing of this structure. Note that this is a continuous-gate structure. In this structure the drain

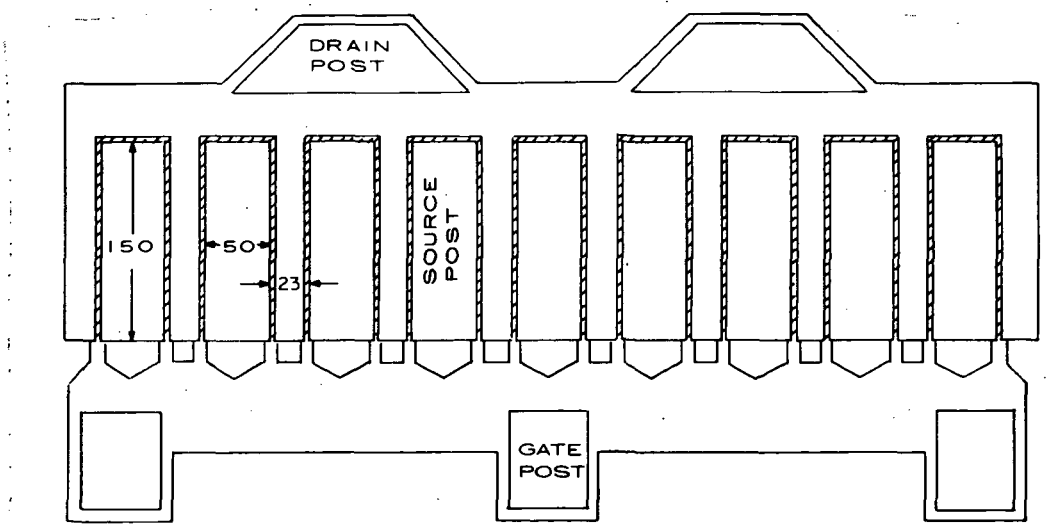


Figure 76. 2-W continuous-gate FET. Pellet size is 707 x 400 μm.

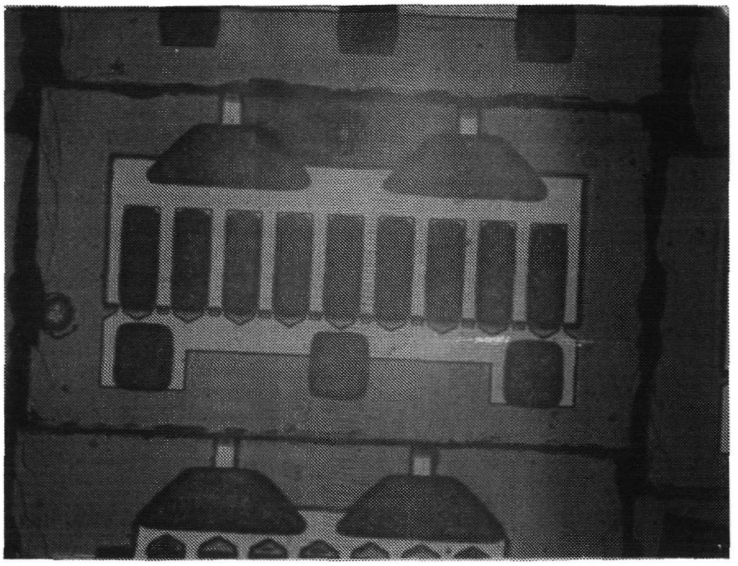
ends of two adjacent gate stripes are connected by another 50-μm gate element. This makes more effective use of the GaAs real estate and also equalizes signal

phase at the drain end of the connected gate stripes. Figure 77 shows photographs of both continuous and open gate FETs. We have found that statistically the continuous gate structure outperforms the open gate structure in terms of gain, output power, and power-added efficiency.

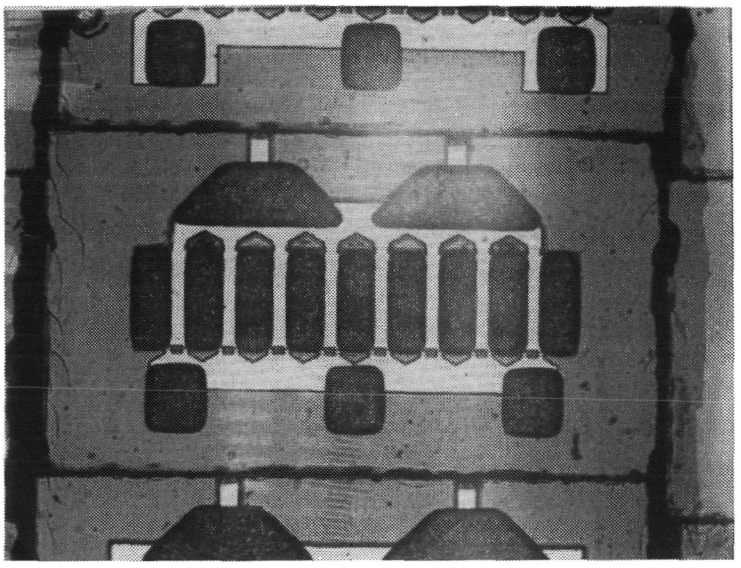
Figure 78 shows the calculated equivalent circuit of an 18-gate FET; Table 21 shows the corresponding S-parameters. We partially match each 18-gate cell before combining. CAD shows that a series stub with 15-Ω impedance and a length of 40° (at 14 GHz) at the input, and 22 Ω with 50° length (14 GHz) at the output forms an adequate partial match. Table 22 shows the S-parameters of the partially matched 18-gate FET. S_{11} and S_{22} are plotted in Figs. 79 and 80, respectively. At band center, the input and output impedances of this partially matched FET are nearly 250 Ω. S_{11} and S_{22} of three such cells paralleled at these reference planes are shown in Figs. 81 and 82, respectively. Note that the impedance swing over the 12- to 16-GHz range is more tractable.

4. Implementation

The partially impedance-matched FET shown in Fig. 83 can be fabricated using a self-aligned gate technique or an alignment technique. The combination of the three cells can be achieved by (a) using a specially designed package, as shown in Fig. 83 or (b) combining the three cells on the GaAs chip by photolithographic technique. Thus, the single GaAs FET chip is a monolithic power amplifier which is a combination of three unit cells. Each unit cell is impedance-matched or partially matched before the combination. The fabrication process of such a monolithic amplifier is no more complicated than the fabrication process of a regular, discrete FET. A schematic diagram of a single-cell, 18-gate FET design is shown in Fig. 84. The sizes of the drain pad, drain line, gate pad, and gate line are designed to form low pass filter matching networks to partially match the drain and the gate impedances, respectively (see Fig. 72). The gate pad width is 650 μm which corresponds to a line impedance of about 15 Ω. The drain pad width is 500 μm corresponding to a 20-Ω line impedance. Gold posts are plated onto the source, gate, and drain pads to allow flip-chip mounting to the specially designed carrier.

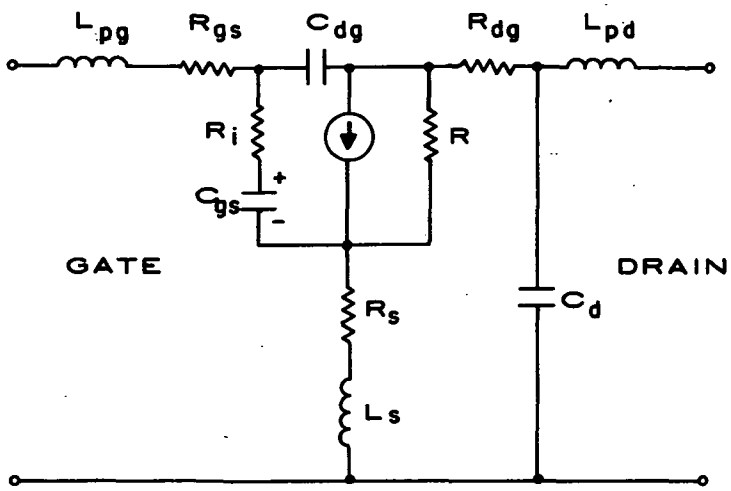


(a)



(b)

Figure 77. Photographs of (a) continuous-gate power FET and (b) regular-gate FETs. Saw marks of dicing saw are visible around the FET pellet.



L_{pg}	= 0.25 nH	R_{gs}	= 1.29 Ω	C_{dg}	= 0.16 pF
R_i	= 0.69 Ω	C_{gs}	= 2.34 pF	g_m	= 247 mS
R_o	= 195 Ω	R_{dg}	= 0.69 Ω	L_{pd}	= 0.1 nH
R_s	= 0.2 Ω	L_s	= 0.01 nH	C_d	= 1.3 pF

Figure 78. Calculated equivalent circuit of 18-gate (continuous-gate) RCA FET.

TABLE 21. CALCULATED S-PARAMETERS OF AN 18-GATE CONTINUOUS-GATE FET

TITLE:
DATA FILE: JG1

FREQ	S11		S21		S12		S22		STAB	
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	K	GMAX
12000.	.906	147.3	.412	-19.7	.018	-93.6	.932	155.4	.989	.000
12500.	.908	145.2	.378	-22.5	.017	-95.6	.943	152.9	1.038	12.25
13000.	.911	143.2	.348	-25.2	.016	-97.5	.947	150.5	1.089	11.51
13500.	.913	141.2	.321	-27.8	.015	-99.3	.951	148.2	1.141	10.93
14000.	.915	139.2	.296	-30.3	.014	-101.	.955	145.9	1.194	10.44
14500.	.917	137.3	.274	-32.8	.014	-102.	.958	143.7	1.249	10.00
15000.	.919	135.5	.255	-35.1	.013	-104.	.961	141.6	1.305	9.606
15500.	.921	133.6	.236	-37.4	.012	-105.	.964	139.5	1.363	9.238
16000.	.923	131.8	.220	-39.7	.012	-107.	.966	137.4	1.423	8.893

TABLE 22. S-PARAMETERS OF A PARTIALLY MATCHED 18-GATE FET. INPUT MATCHING = 15 ohm, 40° (at 14 GHz) SERIES STUB. OUTPUT MATCHING = 22 ohm, 50° (at 14 GHz) SERIES STUB

PART. MATCH. 15 OHM 40 D,29 OHM 50 D

FREQ	S11		S21		S12		S22		STAB	
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	K	GMAX
12000.	.666	67.40	1.279	-162.	.031	76.79	.883	-76.79	.985	.000
12500.	.643	49.98	1.274	-177.	.031	69.09	.868	-68.85	1.035	12.30
13000.	.632	29.65	1.246	164.	.031	62.43	.851	-61.67	1.087	11.52
13500.	.635	9.088	1.182	149.	.031	56.03	.844	-55.65	1.138	10.96
14000.	.654	-11.2	1.086	136.	.031	50.44	.857	-50.44	1.191	10.46
14500.	.684	-29.7	.966	126.0	.031	45.57	.884	-47.59	1.240	10.06
15000.	.720	-45.5	.835	119.9	.031	42.13	.915	-48.13	1.302	9.621
15500.	.759	-60.2	.703	146.0	.031	70.42	.678	-40.2	1.357	9.266
16000.	.794	-72.4	.582	132.3	.031	65.09	.897	-54.5	1.427	8.874

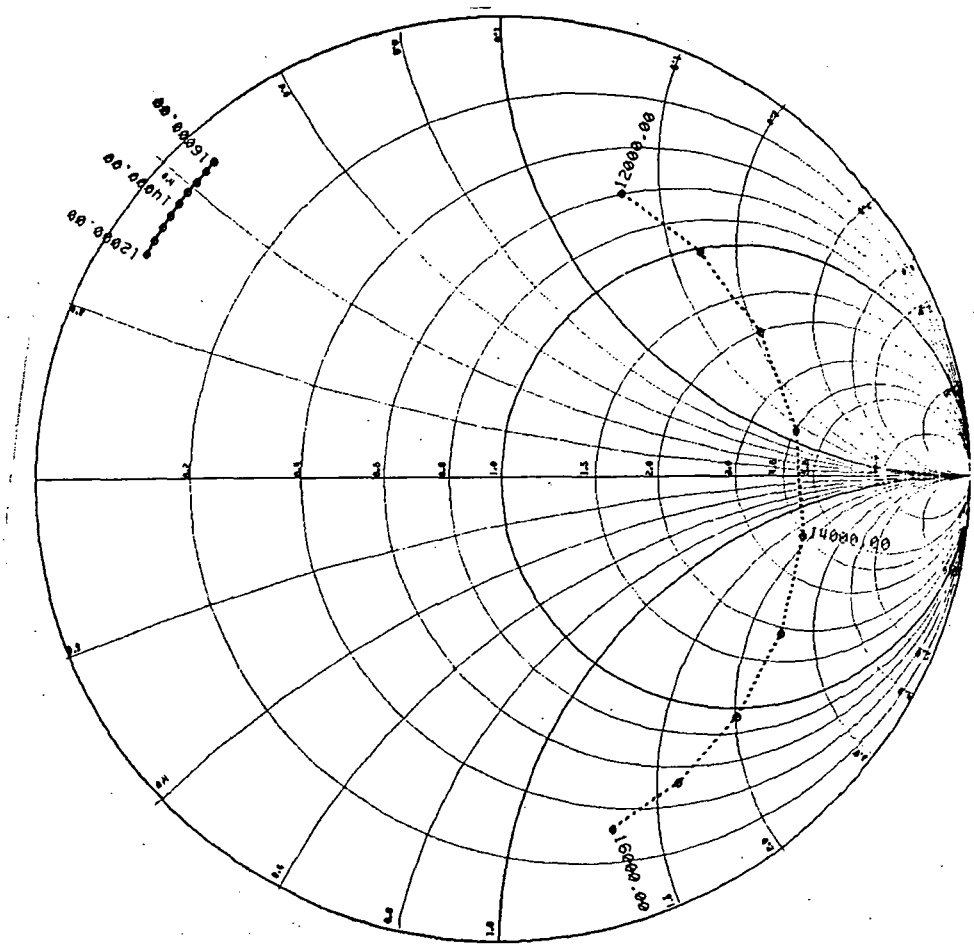


Figure 79. S_{11} plot of a partially matched 18-gate FET.

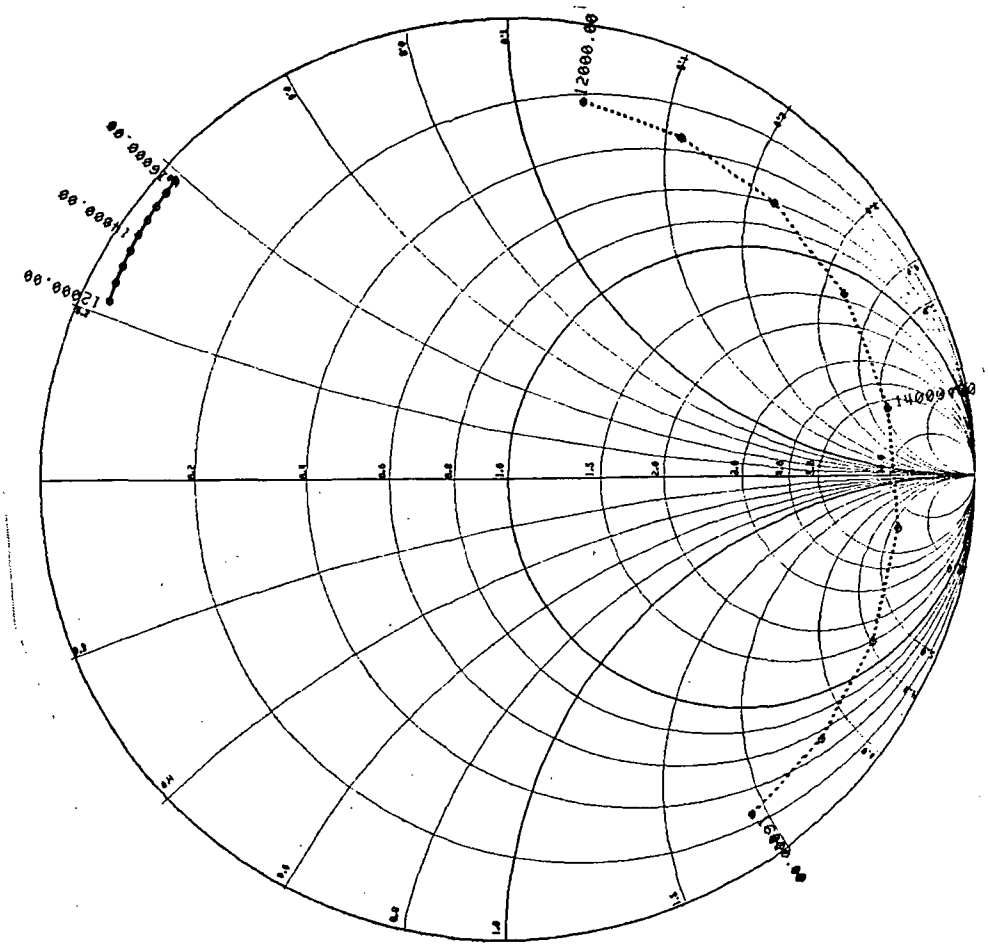


Figure 80. S_{22} plot of a partially matched 18-gate FET.

To achieve 3.5-W output power, we combine three of the partially impedance-matched 18-gate FET cells, as shown in Fig. 85. The 3-cell pellet size is about 2.54x0.6 mm. A specially designed carrier package was shown in Fig. 83 to facilitate the flip-chip mounting of the 3-cell FET pellet onto the carrier package. Note that each gate and drain pad will be connected to low impedance transmission lines. The input lines are paralleled after 40° at band center (14 GHz) and the output lines paralleled after about 50° (14 GHz). The accurate dimensions can be determined by a complete design analysis and computer

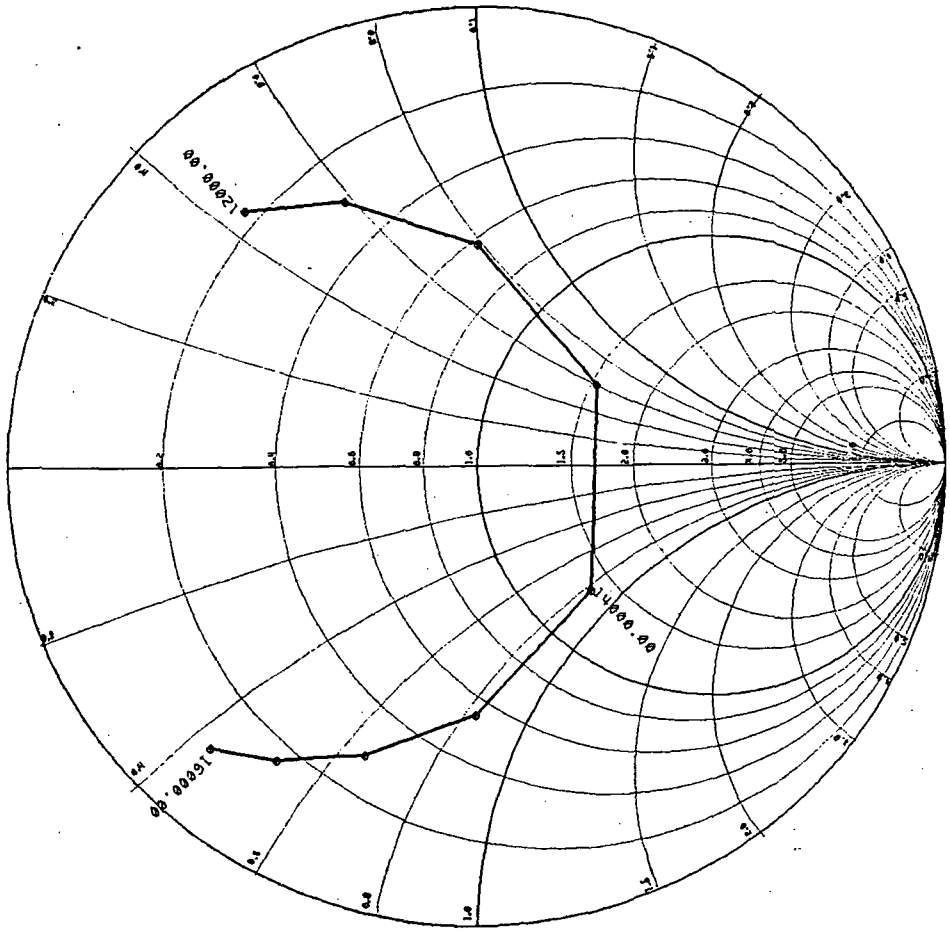


Figure 81. Calculated S_{11} plot of a combined FET with three partially matched 18-gate FETs in parallel.

simulation. Note that the FET can be mounted in one operation and no wire bonding is involved. This is only possible if the unique flip-chip FET approach pioneered by RCA is used. With this design the inactive zone is minimized. Also, since the individual cells are impedance-matched before

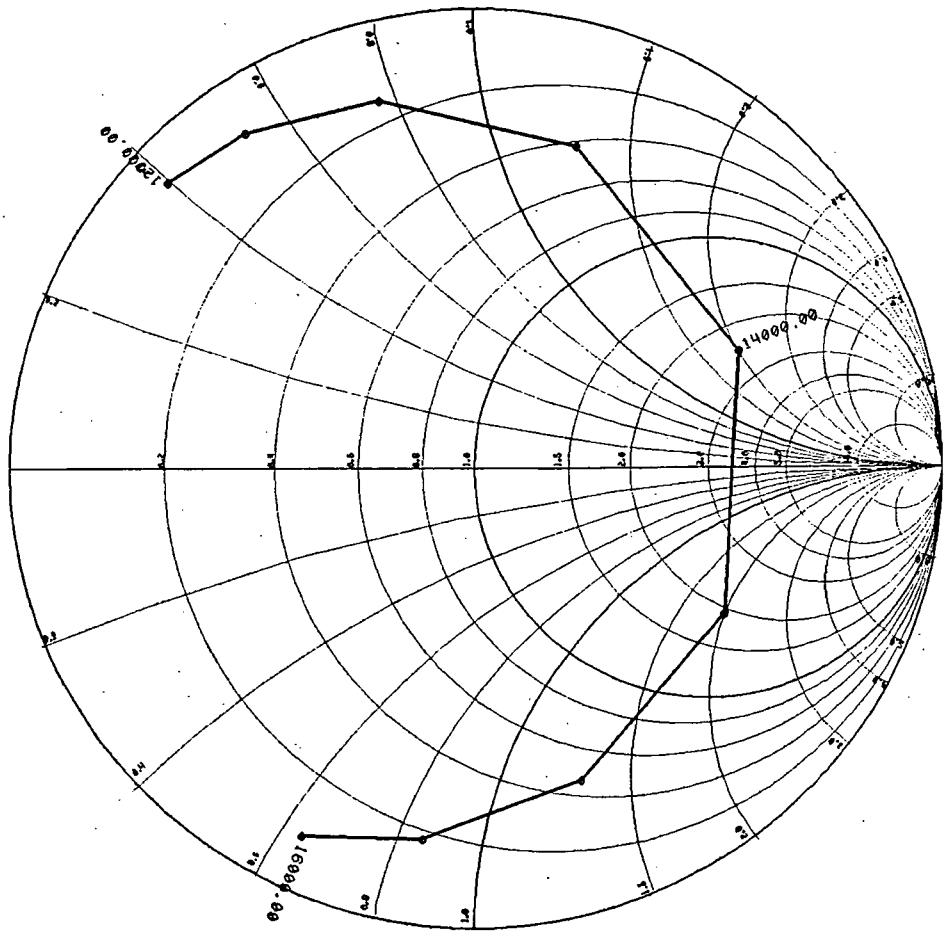


Figure 82. S_{22} plot of a combined FET with three partially matched 18-gate FETs in parallel.

combination, the impedance of the combined 3-cell, 3.5-W FET remains reasonably high and it can be matched to the 50-ohm without excessive loss.

I. SUMMARY OF RF DEVICE PERFORMANCE

In this section we report the results of small-signal S-parameter measurements up to 12 GHz and power gain measurements up to 15 GHz on selected wafers.

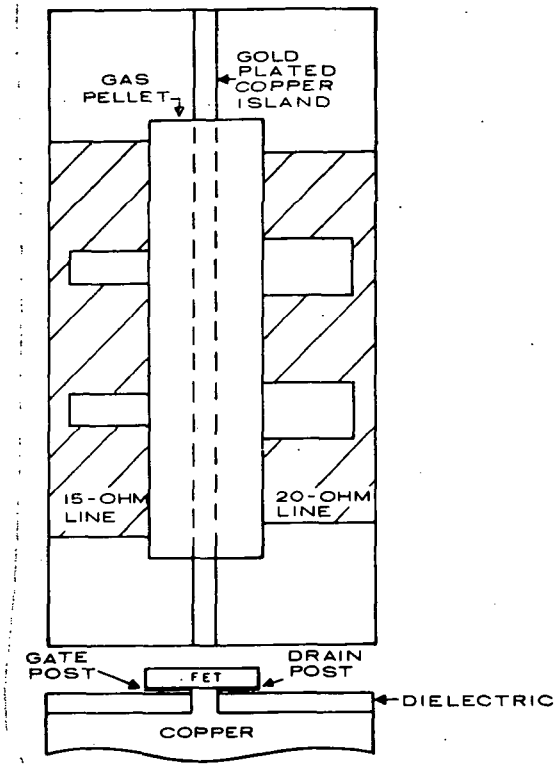


Figure 83. Schematic diagram of the proposed flip-chip-mounted FET.

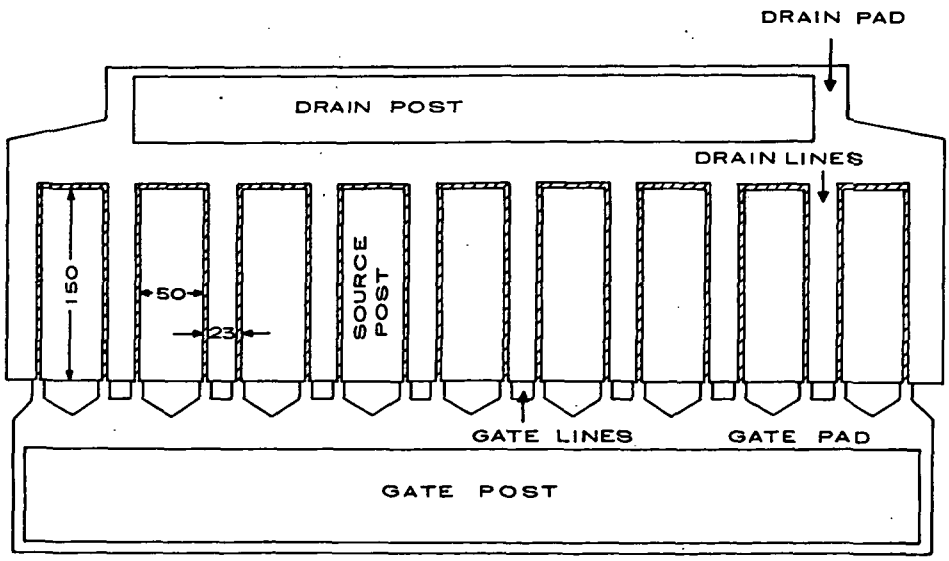


Figure 84. Unit cell of an 18-gate (continuous-gate) FET. A pellet will consist of three such cells. Pellet size is 2.54 x 0.6 mm.

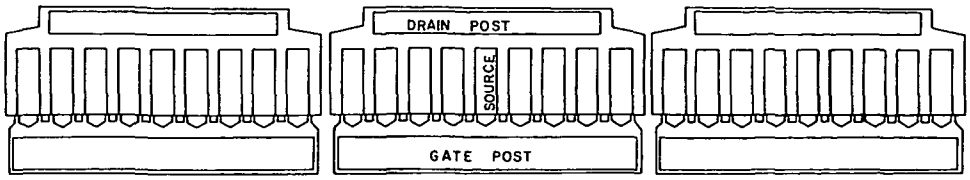


Figure 85. Design of a 3-cell FET for 3.5-W output power in Ku-band. Each cell is partially impedance matched.

The bulk of the devices tested were fabricated by the self-aligned gate process. The aligned-gate process was being developed during this period and only resulted in a few useful device wafers. Nearly all the wafers processed were grown by vapor-phase epitaxy and contained n^+ capping layers. A few of the wafers had an undoped buffer layer grown in situ prior to active layer growth, but most were grown directly on a semi-insulating substrate. Two wafers produced by ion implantation into semi-insulating substrates were processed by the aligned-gate process.

Table 23 presents the power gain characteristics of a device from wafer A105. This wafer had a 4.5-μm undoped high-resistivity buffer layer and was processed to make 18-gate FETs. Because of the relatively low gain, the devices were tested at 10 GHz. The performance at 10 GHz was 5.0-dB small-signal gain; 1.26-W output power with 3.9-dB power gain; and 11.8% power-added efficiency.

Much better performance was exhibited by wafer C182. Wafer C182 did not have a highly doped n^+ capping layer, so AuGe/Ni metallization was used for the ohmic contacts. An 8-gate, continuous-gate FET from this wafer had 4.5-dB small-signal gain, 743-mW output power with 3.1-dB power gain and 19% power-added efficiency of 15 GHz. Table 24 shows the detailed power gain characteristics measured at 15 GHz.

These two wafers exemplify a general relationship between I_D-V_D characteristics and rf performance. During the course of FET evaluations, we noticed that the I_D-V_D characteristics of all the good performance FETs showed a triode-like characteristic. When the drain voltage is greater than the saturation voltage, the drain current increase slightly with increasing drain

TABLE 23. P_{in}-P_{out} CHARACTERISTICS OF AN 18-GATE CONTINUOUS-GATE FET FROM WAFER A105 at 10 GHz

DEVICE: A105-1 18 CG

V_D = 10 V, I_{DSSO} = 1000 mA, V_G = -2 V, f = 10 GHz

P_{in}(mW)	P_{out}(mW)	G(dB)	I_D(mA)	P_{out}-P_{in}(mW)	η_{PA}(%)
86	263.2	4.9	609		
172	539	5.0	623		
258	798	4.9	642		
344	1022	4.7	653		
436	1162	4.3	644		
516	1262	3.9	632	746	11.8%
602	1316	3.4	622	714	11.5%

TABLE 24. P_{in}-P_{out} CHARACTERISTICS OF AN 8-GATE CONTINUOUS-GATE FET FROM WAFER C182 AT 15 GHz

V_D = 9 V

P_{in}(mW)	P_{out}(mW)	I_D(mA)	Gain(dB)	η_{PA}(%)
181	514	229	4.5	
225	612	230	4.3	
271	683	230	4.0	19.9
317	722	229	3.6	19.7
362	743	228	3.1	18.6

voltage. This type of I_D-V_D characteristic is exhibited by devices from wafer C182, as shown in Fig. 86. The drain current, I_D, initially decreases at around 2 to 4 V of drain voltage. We attribute this current drop to be probably related to the Gunn effect. After this initial decrease, I_D increases slightly with increasing drain voltage. The dc transconductance also exhibits an initial drop, and then increases slightly with increasing drain voltage. In contrast to C182, FETs from wafer A105 showed a decreasing drain current with increased drain voltage, as shown in Fig. 87. The transconductance also decreases with increasing V_D after the onset of current saturation. The difference in the I_D-V_D characteristics is attributed to the difference in the drift mobility of the n layer to semi-insulating layer interface.

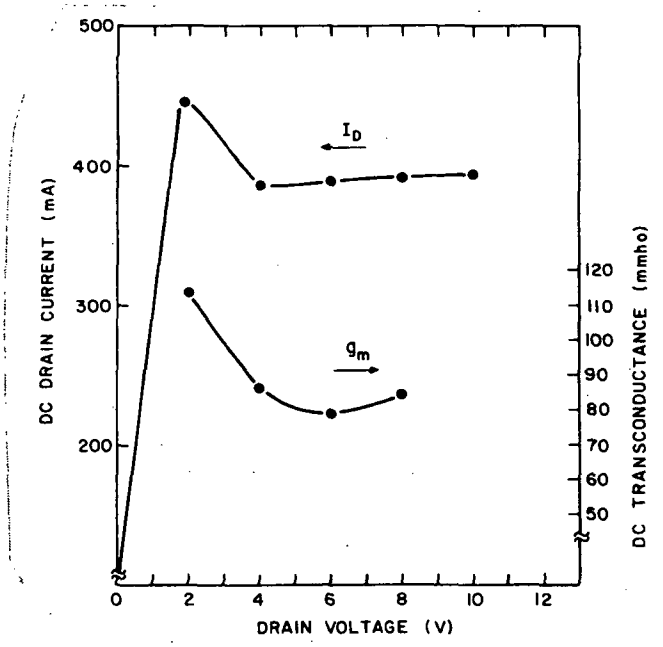


Figure 86. I_D and g_m vs V_D for an 8-gate regular gate FET from C182.

The S-parameters of FETs from wafer C182 were measured also in the Ku-band frequencies. Table 25 shows the S-parameters of device C182B-89 from 11 to 16 GHz. The input (S_{11}) and output (S_{22}) impedances are fairly well behaved, which is indicative of reasonably good measurement accuracy. Table 26 shows the small-signal gain of the same FET. The maximum available gain, Ga, is 9 dB at 12.5 GHz and 5.0 dB at 15.5 GHz. The measured Ga agrees well with the data from the power measurement. S_{11}, S_{22}, and Ga of this FET are plotted in Figs. 88, 89, and 90, respectively.

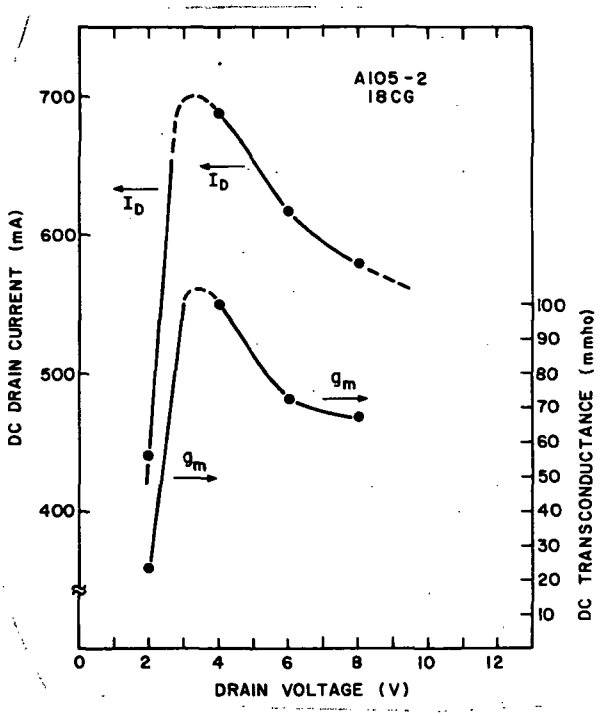


Figure 87. I_D and g_m vs V_D for A105-2. This wafer has a 4.5-μm undoped high-resistivity layer.

Wafer B995 was processed to form 18-gate FETs with AuGe/Ni/Ti/Pt/Au ohmic contacts. This wafer did not have a buffer layer. Table 27 shows the measured performance of an FET at 15 GHz. The B995 FET has a small-signal gain of 2.6 dB and an output power of 556 mW at 1-dB compression point with a power-added efefficiency of 3.8%. These results are quite far from the design goals. The poor performance may reflect problems that were encountered in thermal compression bonding of devices from wafer B995. To investigate the quality of the chip attachment to the mounting stub, we measured the operation temperature of the device. Figure 91 shows that the operation temperature varied from 80°C at one end of the chip to 130°C at the other end.

Wafer D147 consists of an n-layer grown directly on a semi-insulating substrate. It does not have either a buffer layer or an n^+ contact layer. Wafer D147 was processed with the 18-gate FET mask set and has AuGe/Ni/Ti/Pt/Au ohmic contacts. The first FET from D147 showed a small-signal gain of 3.3 dB and an output power of 675 mW at 1-dB compression point with a power-added efficiency of 5.5% at 15 GHz. The power gain characteristics of device D147-5 are given in Table 28. A second device from this wafer D147-14 showed 1.05-W output power at 15 GHz with 8.6% power-added efficiency. The small-signal gain of this FET was 3.5 dB and the power gain was 2 dB (including circuit losses).

TABLE 25. S-PARAMETERS OF C182B-89

GOEL-DORNAN TEST REPORT
C-182B

.00 VOLTS, .00 MA (MEAS 1) #89 V_D V_G I_D 8.0,-2.0,35.0MA

FREQ (MHZ)	S11 MAG	S11 ANG	S21 MAG	S21 ANG	S12 MAG	S12 ANG	S22 MAG	S22 ANG
11000.00	.959	178	.916	6	.059	-32	.711	-137
11100.00	.957	177	.928	6	.059	-33	.713	-138
11200.00	.957	177	.948	4	.060	-33	.729	-138
11300.00	.977	177	.943	2	.060	-34	.734	-139
11400.00	.973	177	.909	1	.058	-34	.740	-139
11500.00	.976	177	.891	0	.058	-35	.749	-139
11600.00	.970	176	.900	0	.057	-35	.755	-139
11700.00	.970	175	.905	-2	.058	-35	.758	-139
11800.00	.974	175	.891	-3	.057	-36	.766	-140
11900.00	.966	175	.881	-4	.057	-36	.769	-139
12000.00	.967	175	.870	-5	.056	-37	.771	-139
12100.00	.960	175	.860	-5	.056	-36	.777	-139
12200.00	.952	175	.857	-6	.056	-36	.769	-139
12300.00	.954	174	.862	-7	.056	-37	.768	-140
12400.00	.955	174	.852	-8	.055	-38	.775	-140
12500.00	.876	173	.804	-9	.054	-39	.731	-140
12600.00	.878	173	.809	-10	.053	-39	.735	-140
12700.00	.872	172	.802	-11	.053	-39	.742	-141
12800.00	.867	172	.799	-11	.053	-39	.734	-141
12900.00	.863	171	.794	-12	.052	-39	.730	-142
13000.00	.858	171	.794	-13	.053	-40	.737	-143
13100.00	.851	170	.789	-14	.052	-40	.731	-143
13200.00	.855	170	.795	-15	.052	-41	.725	-144
13300.00	.850	169	.792	-17	.052	-42	.722	-144
13400.00	.844	168	.777	-18	.051	-42	.714	-144
13500.00	.838	168	.771	-18	.050	-42	.712	-145
13600.00	.838	168	.769	-19	.050	-43	.713	-145
13700.00	.832	167	.767	-20	.050	-42	.708	-145
13800.00	.818	166	.772	-21	.050	-42	.696	-144
13900.00	.809	165	.772	-23	.051	-44	.696	-144
14000.00	.809	165	.741	-25	.049	-45	.705	-144
14100.00	.805	164	.729	-24	.048	-45	.702	-145
14200.00	.807	163	.732	-25	.048	-44	.700	-146
14300.00	.815	163	.731	-25	.047	-44	.697	-147
14400.00	.805	161	.741	-26	.048	-44	.688	-148
14500.00	.809	161	.752	-28	.049	-45	.684	-148
14600.00	.807	160	.737	-29	.048	-46	.677	-150
14700.00	.803	159	.724	-29	.047	-45	.667	-150
14800.00	.814	158	.722	-30	.046	-45	.668	-151
14900.00	.810	158	.725	-31	.046	-46	.664	-151
15000.00	.810	156	.704	-32	.045	-45	.662	-152
15100.00	.818	156	.698	-33	.045	-45	.667	-153
15200.00	.814	155	.705	-32	.045	-44	.668	-154
15300.00	.810	154	.706	-34	.046	-45	.662	-155
15400.00	.822	154	.696	-34	.044	-45	.665	-157
15500.00	.821	154	.735	-35	.047	-46	.663	-158
15600.00	.834	151	.720	-41	.044	-49	.653	-160
15700.00	.831	150	.677	-41	.042	-48	.654	-161
15800.00	.835	149	.671	-42	.043	-47	.654	-162
15900.00	.840	148	.667	-41	.043	-47	.655	-164
16000.00	.846	148	.664	-42	.042	-47	.655	-166

TABLE 26. GAIN OF C182B-89

KU AMP.
GOEL-DORNAN TEST REPORT
C-182B

.00 VOLTS, .00 MA (MEAS 1) #89 8.0,-2.0,350MA

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
11000.00		13.21	-.76	-24.54	.14	.92
11100.00		13.19	-.65	-24.58	.13	.90
11200.00			-.46	-24.39	.03	1.34
11300.00			-.51	-24.50	-.01	1.93
11400.00			-.83	-24.69	.04	1.58
11500.00			-1.00	-24.77	.00	1.83
11600.00			-.91	-24.81	.04	1.49
11700.00			-.87	-24.80	.05	1.54
11800.00			-1.00	-24.85	.03	1.79
11900.00			-1.10	-24.90	.13	1.38
12000.00			-1.21	-25.03	.13	1.38
12100.00			-1.31	-25.05	.17	1.16
12200.00		12.81	-1.34	-25.05	.26	.91
12300.00		13.01	-1.29	-25.06	.25	.95
12400.00		13.16	-1.39	-25.14	.27	.99
12500.00	9.28	7.78	-1.89	-25.37	1.17	.26
12600.00	9.50	7.93	-1.84	-25.44	1.14	.26
12700.00	9.15	7.76	-1.92	-25.50	1.19	.26
12800.00	8.66	7.47	-1.95	-25.58	1.28	.23
12900.00	8.21	7.20	-2.00	-25.61	1.36	.22
13000.00	8.18	7.19	-2.01	-25.59	1.37	.22
13100.00	7.69	6.87	-2.06	-25.65	1.48	.20
13200.00	7.74	6.94	-2.00	-25.62	1.47	.20
13300.00	7.39	6.75	-2.03	-25.71	1.57	.19
13400.00	6.85	6.32	-2.20	-25.86	1.73	.17
13500.00	6.53	6.07	-2.26	-25.98	1.85	.16
13600.00	6.25	5.86	-2.28	-26.00	1.96	.15
13700.00	6.22	5.82	-2.31	-26.01	1.97	.15
13800.00	5.77	5.43	-2.25	-25.95	2.15	.13
13900.00	5.46	5.24	-2.24	-25.90	2.28	.12
14000.00	5.14	4.99	-2.61	-26.15	2.41	.12
14100.00	4.92	4.74	-2.74	-26.39	2.55	.11
14200.00	5.01	4.79	-2.71	-26.41	2.52	.11
14300.00	5.14	4.90	-2.72	-26.48	2.46	.11
14400.00	4.96	4.70	-2.61	-26.36	2.56	.11
14500.00	5.11	4.87	-2.48	-26.26	2.49	.11
14600.00	4.79	4.59	-2.65	-26.43	2.66	.10
14700.00	4.45	4.25	-2.80	-26.62	2.87	.09
14800.00	4.67	4.44	-2.83	-26.72	2.76	.10
14900.00	4.59	4.37	-2.80	-26.71	2.82	.09
15000.00	4.29	4.08	-3.05	-26.98	3.01	.09
15100.00	4.49	4.23	-3.13	-26.98	2.86	.09
15200.00	4.54	4.24	-3.04	-26.85	2.81	.09
15300.00	4.41	4.13	-3.02	-26.84	2.90	.09
15400.00	4.57	4.27	-3.15	-27.05	2.82	.09
15500.00	5.05	4.70	-2.68	-26.61	2.56	.10
15600.00	5.01	4.74	-2.63	-27.06	2.67	.10
15700.00	4.40	4.14	-3.32	-27.49	3.00	.09
15800.00	4.46	4.16	-3.46	-27.41	2.91	.09
15900.00	4.63	4.24	-3.51	-27.40	2.78	.09
16000.00	4.76	4.34	-3.56	-27.47	2.71	.10

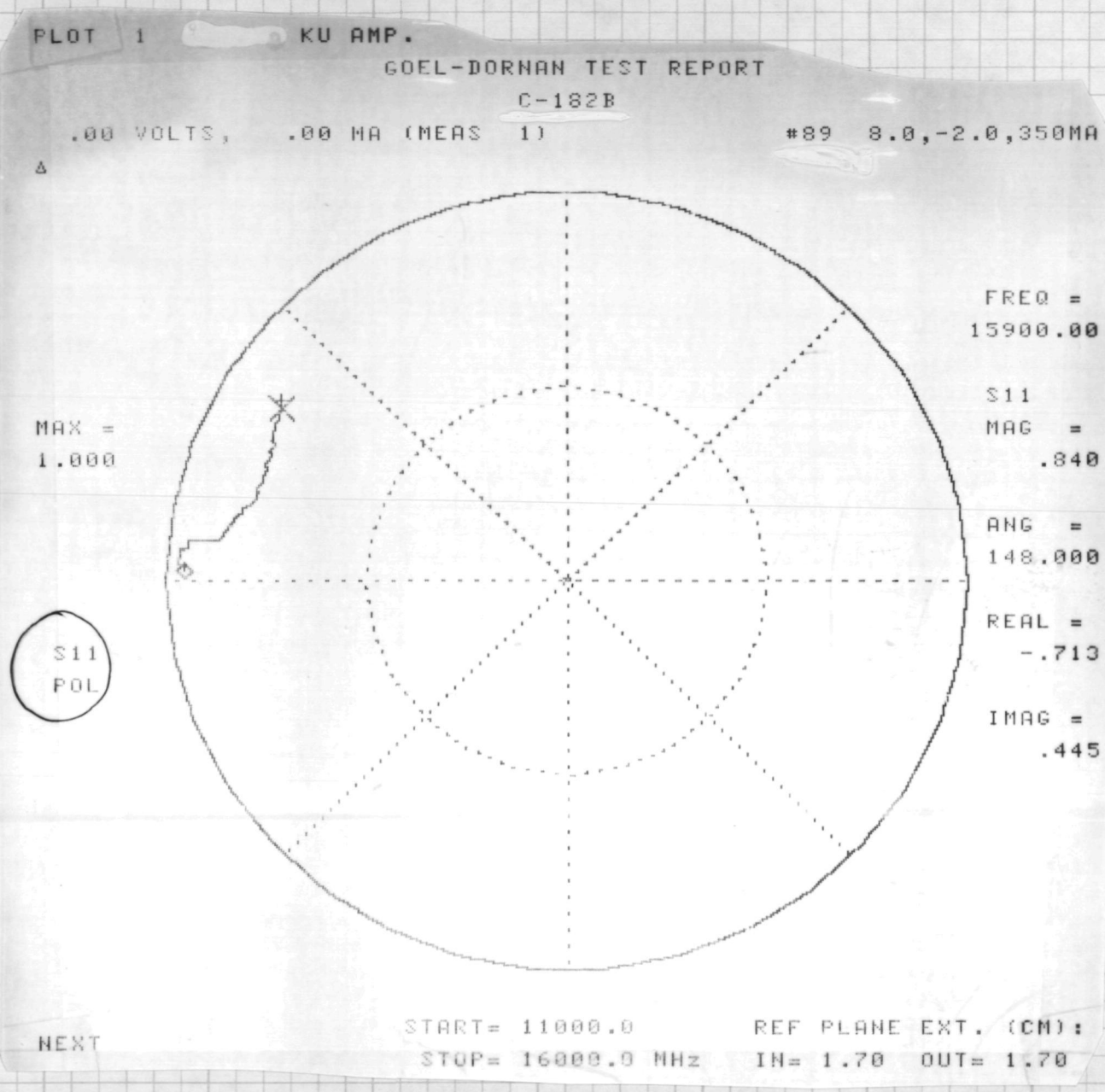


Figure 88. S_{11} plot of C182B-89.

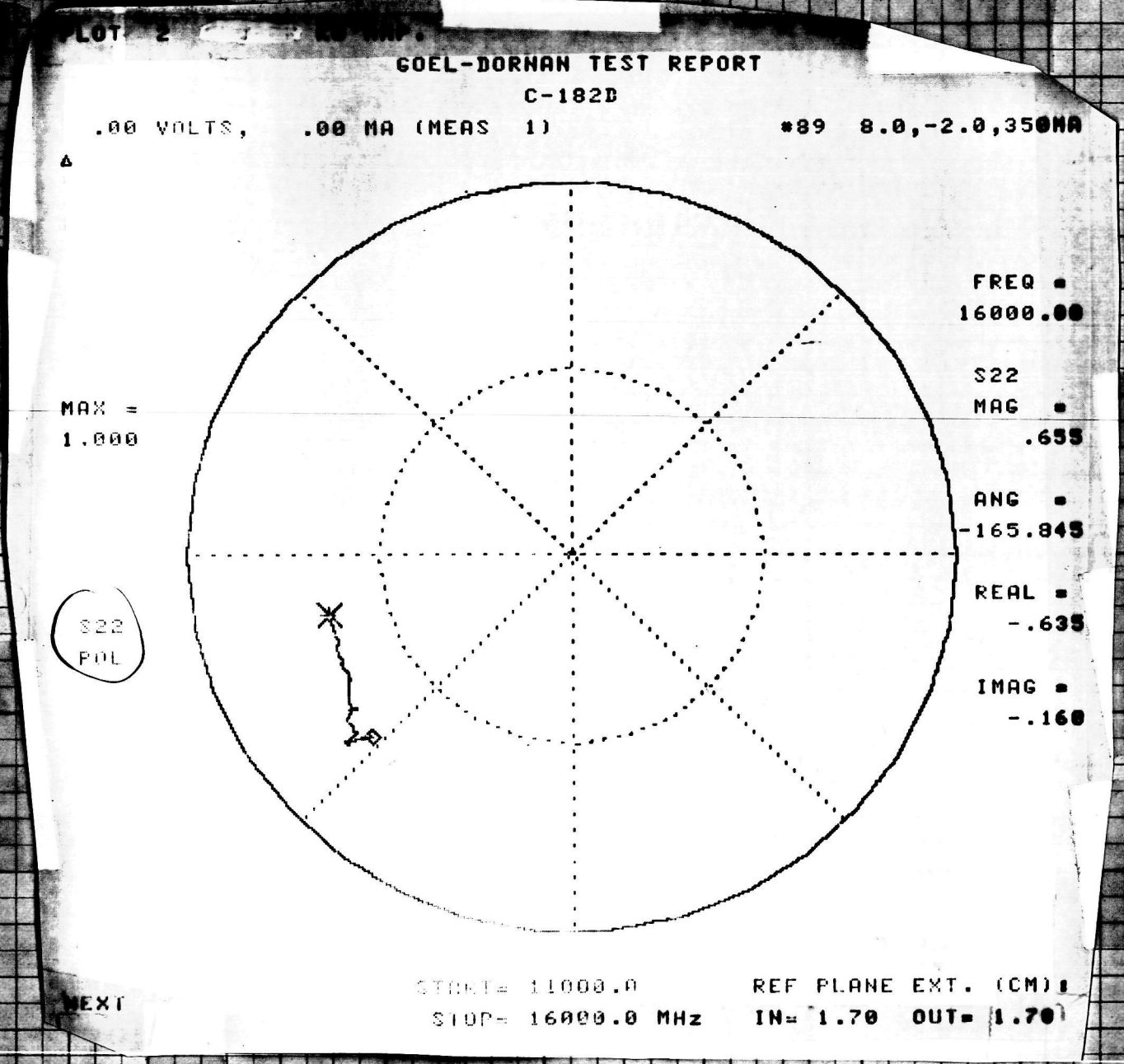


Figure 89. S_{22} plot of C182B-89.

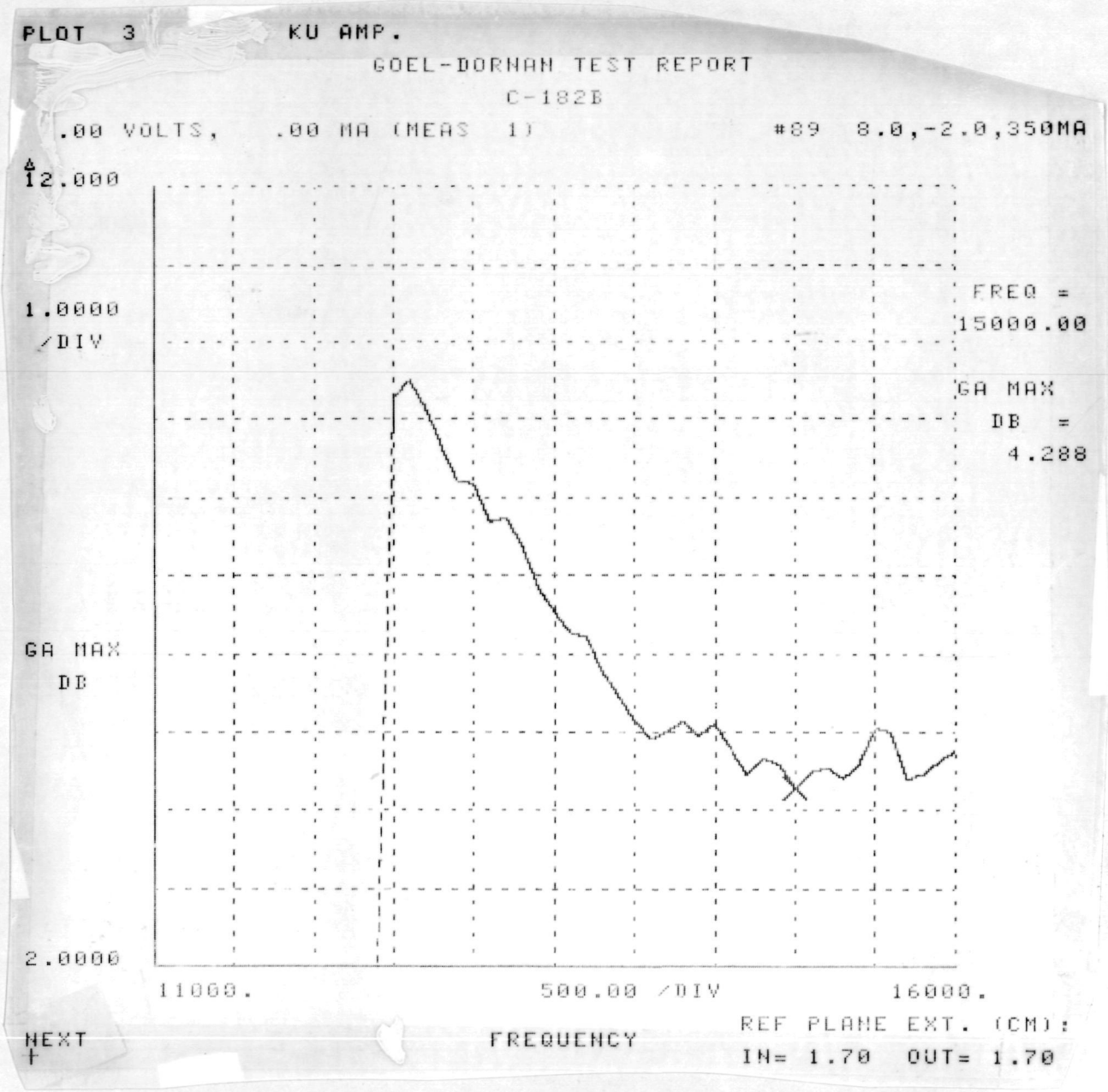


Figure 90. Ga of C182B-89.

TABLE 27. P_{in}-P_{out} CHARACTERISTICS OF AN 18-GATE CONTINUOUS-GATE FET FROM WAFER B995 AT 15 GHz

V_D = 5 V, V_G = -1 V, f = 15 GHz

P_{in}(mW)	P_{out}(mW)	G(dB)	I_D(mA)	P_{out}-P_{in}(mW)	η_{PA}(%)
78.5	136.85	2.4	1013		
157.0	283.22	2.6	1032		
235.5	389.13	2.2	1042	153.63	3.69
314.0	483.14	1.9	1053	169.14	4.0
392.5	555.73	1.5	1060	163.23	3.85

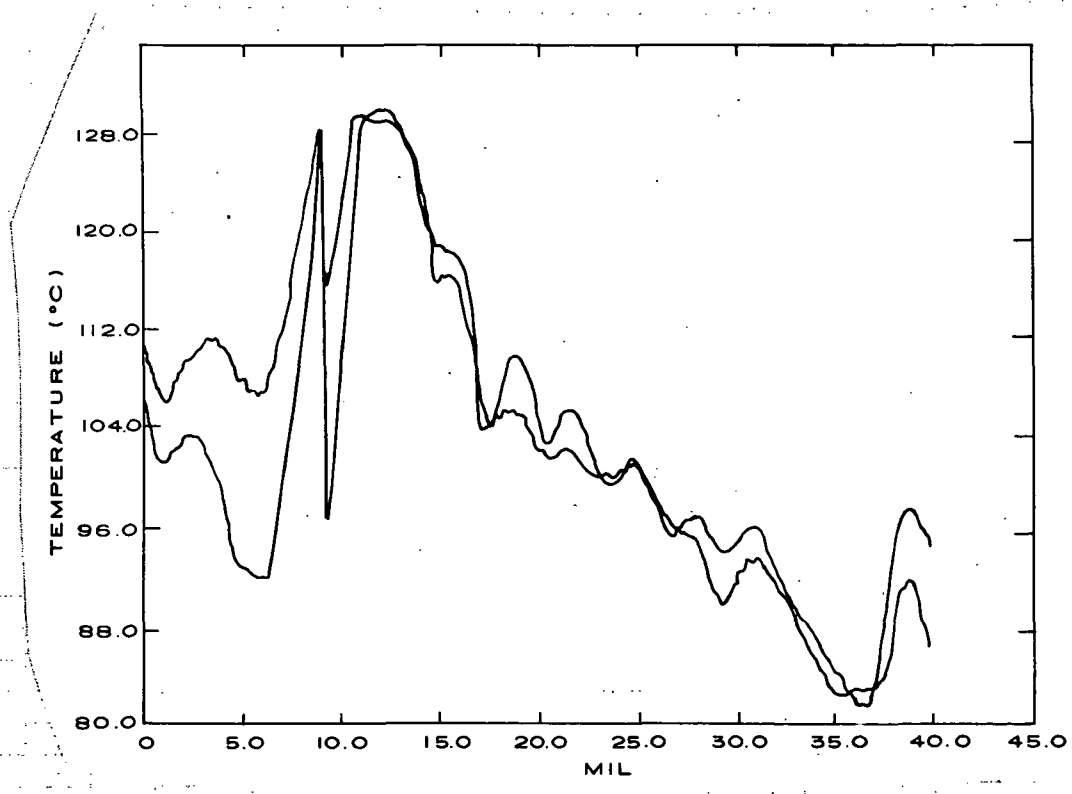


Figure 91. Temperature profile of FET from wafer B995.

TABLE 28. P_{in}-P_{out} CHARACTERISTICS OF AN 18-GATE CONTINUOUS-GATE FET WAFER D147

V_D = 8 V, I_{DSSO} = 890 mA, V_G = -1 V, f = 15 GHz

P_{in}(mW)	P_{out}(mW)	G(dB)	I_D(mA)	P_{out}-P_{in}(mW)	η_{PA}(%)
157	161.8	3.1	615		
236	339	3.3	672		
314	506	3.3	648		
393	601	2.8	645		5.6
471	675	2.4	644		5.5
	729	1.9	642		
			640		

Table 29 is the P_{in}-P_{out} characteristic of this FET at 15 GHz. D147 is the first wafer run that exhibited 1-W output power at 15 GHz. The gain and efficiency were still below contract goals. Because of significant circuit loss at 15 GHz, the intrinsic device characteristics are somewhat better than the measurement results. We have measured the circuit loss of a test fixture similar to the one used to obtain the rf results in Table 29. We found that the loss of the test fixture was about 0.45 dB at both the input and output. If these losses are taken into account, the D147-14 performance would be 1.17-W output power at 3-dB power gain with 13% power-added efficiency.

Wafer D169 also consisted of an n layer grown directly on a semi-insulating substrate; it had no n^+ contact layer or buffer layer. The gain of devices from this wafer was slightly low but still within our normal performance range. The small-signal gain was about 6 dB at 10 GHz and 5 dB at 12 GHz. The output power of D169-8 was 476 mW with 4.4-dB power gain and 11.5% power-added efficiency at 10 GHz. Table 30 shows the S-parameters of 8-gate FETs from wafer D169. Because of the low gain, power measurements were made at 10 GHz. The power gain measurement results are given in Table 31.

Two other epitaxial layer wafers showed reasonable small-signal gain. Wafer D319 was fabricated with the 16- to 18-gate mask set. The gain, power

TABLE 29. P_{in}-P_{out} CHARACTERISTICS OF AN 18-GATE CONTINUOUS-GATE FET FROM WAFER D147

DEVICE: D147-14 18 CG

V_D = 7.6, V_G = -1.1 V, f = 15 GHz

P_{in}(mW)	P_{out}(mW)	G(dB)	I_D(mA)	P_{out}-P_{in}(mW)	η_{PA}(%)
41.5	93.6	3.5	570		
83	187.2	3.5	566		
166	353.6	3.3	569		
332	629.2	2.8	577		
498	871.0	2.4	584	373	8.4%
581	969.8	2.2	589	388	8.7%
664	1049.1	2.0	591	385	8.6%
747	1110	1.7	579	363	8.3%

TABLE 30. S-PARAMETERS OF 8-GATE FETs FROM WAFER D169

D169-8(RG) -2,8.0,390MA JUNE 13, 1978

FREQ	S11		S21		S12		S22	
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
8000.0	.818	-156.9	.987	33.0	.051	-9.1	.564	-122.7
8500.0	.820	-157.7	.941	29.0	.046	-8.4	.590	-124.8
9000.0	.830	-160.9	.901	23.9	.045	-8.2	.612	-127.8
9500.0	.826	-166.0	.862	19.2	.045	-8.9	.630	-129.9
10000.0	.813	-172.3	.826	13.1	.043	-10.2	.649	-132.9
10500.0	.660	175.6	.715	7.0	.039	-9.6	.662	-135.6
11000.0	.689	-159.5	.693	12.5	.039	-1.5	.671	-138.9
11500.0	.807	-169.8	.705	3.8	.039	-6.4	.662	-139.1
12000.0	.843	-176.4	.689	-.7	.036	-5.6	.667	-143.1

REFL PLANES: 2.50 1.70 TRAN LIN: 4.20

D169-8(RG) -2,8.0,390MA JUNE 13, 1978

FREQ	MASON	MSG	MAG	MUG	GO	G1	G2	K	DELTA
8000.0	8.52	12.86	7.14	6.36	-.11	4.81	1.67	2.00	.44
8500.0	8.19	13.10	6.86	6.17	-.53	4.85	1.86	2.23	.46
9000.0	8.54	12.99	6.97	6.19	-.90	5.06	2.04	2.13	.49
9500.0	8.26	12.85	6.68	5.89	-1.29	4.99	2.20	2.19	.50
10000.0	7.52	12.83	6.10	5.40	-1.66	4.69	2.37	2.46	.51
10500.0	2.70	12.68	2.35	2.08	-2.91	2.49	2.50	5.44	.42
11000.0	2.24	12.51	1.95	1.73	-3.16	2.28	2.60	5.73	.41
11500.0	5.49	12.55	4.52	4.04	-3.04	4.58	2.50	3.25	.52
12000.0	6.58	12.86	5.35	4.69	-3.24	5.37	2.56	2.90	.55

REFL PLANES: 2.50 1.70 TRAN LIN: 4.20

TABLE 31. P_{in}-P_{out} CHARACTERISTICS OF AN 8-GATE REGULAR-GATE FET FROM WAFER D169 AT 10 GHz

DEVICE: D169-8 8 RG

V_D = 8 V, V_G = -2 V, f = 10 GHz

P_{in}(mW)	P_{out}(mW)	G(dB)	I_D(mA)	P_{out}-P_{in}(mW)	η_{PA}(%)
43	224	7.17	386		
86	347.2	6.06	374		
129	420	5.13	352		
172	476	4.42	332	304	11.45

output, and efficiency of device D319-5 (an 18 continuous gate device) are given in Table 32 at 15 GHz. Wafer C521 was used to fabricate 8-gate devices. The performance of devices at 15 GHz from wafer C521 are presented in Tables 33 and 34.

TABLE 32. P_{in}-P_{out} CHARACTERISTICS OF AN 18-GATE CONTINUOUS-GATE FET FROM WAFER D319 AT 15 GHz

D319-5 18 CG

V_D = 8 V, V_G = -1.5 V, f = 15 GHz

P_{in}(mW)	P_{out}(mW)	G(dB)	I_D(mA)	P_{out}-P_{in}(mW)	η_{PA}(%)
90	197.2	3.4	589		
180	369.75	3.13	598		
270	536.5	2.98	610		
360	667	2.68	625		
450	775.75	2.36	636		
540	884.5	2.14	640	344.5	6.72
630	971.5	1.88	636		
720	1065.75	1.7	633		

TABLE 33. P_{in}-P_{out} CHARACTERISTICS OF AN 8-GATE FET FROM WAFER C521

C521-12 8-Gate FET

V_D = 9.5 V, V_G = -1.95 V, f = 15 GHz

P_{in}(mW)	P_{out}(mW)	G(dB)	I_D(mA)	η_{PA}(%)
43.5	136	5	335	
87	258	4.7	346	
130.5	348	4.7	348	
174	426	3.9	351	7.6
217	453	3.2	348	7.2
261	522	3	345	8

TABLE 34. P_{in}-P_{out} CHARACTERISTICS OF AN 8-GATE FET FROM WAFER C521

C521-16 8-Gate FET

V_D = 9.6 V, V_G = -2 V, f = 15 GHz

P_{in}(mW)	P_{out}(mW)	G(dB)	I_D(mA)	η_{PA}(%)
80	224	4.5		
160	420	4.2		
240	532	3.5	360	8.5
320	665	3.2	366	10.7

In addition to the epitaxial-layer wafers some wafers produced by ion implantation into semi-insulating substrates were used for device fabrication. Because the 250-keV ion-implantation equipment can produce an active device layer only approximately 0.25 μm thick, the ion-implanted wafers were processed by the aligned-gate process. Two processed ion-implanted wafers showed very good S-parameter results. Eight-gate FETs from wafer A28C showed a maximum stable gain (MSG) of 12 dB and a 50 ohm to 50 ohm gain (S_{21} gain) of -1.3 dB at 12 GHz. This small-signal gain performance compares favorably with the

TABLE 35. SMALL-SIGNAL GAIN OF AN 8-GATE FET FROM AN ION-IMPLANTED WAFER

AUG. 16,1978 A 28C -2,8,190

FREQ	S11		S21		S12		S22	
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
4000.0	.980	-125.9	2.367	43.4	.060	-11.4	.721	-119.6
4500.0	.947	-134.7	2.150	30.3	.059	-20.9	.710	-132.7
5000.0	.900	-143.7	1.895	16.7	.057	-30.7	.701	-146.3
5500.0	.909	-149.7	1.734	7.1	.056	-36.0	.709	-157.5
6000.0	.898	-157.9	1.594	-4.3	.056	-42.4	.731	-170.0
6500.0	.895	-163.3	1.507	-13.9	.056	-46.4	.740	179.6
7000.0	.877	-168.6	1.415	-23.2	.055	-51.2	.776	168.1
7500.0	.899	-171.7	1.354	-31.5	.054	-55.0	.771	155.2
8000.0	.906	-178.6	1.303	-43.7	.054	-61.2	.784	141.1
8500.0	.862	177.7	1.245	-55.2	.055	-67.8	.803	127.9
9000.0	.833	173.6	1.177	-66.6	.053	-74.4	.788	115.1
9500.0	.833	171.1	1.114	-76.3	.052	-77.4	.800	102.5
10000.0	.858	166.0	1.079	-88.1	.051	-82.8	.824	88.9
10500.0	.811	157.9	.955	-96.7	.048	-86.4	.837	77.1
11000.0	.821	153.6	.915	-103.1	.046	-86.1	.912	66.4
11500.0	.873	151.0	.913	-114.1	.048	-89.9	.950	53.5
12000.0	.891	145.6	.859	-127.0	.050	-95.6	.922	41.4

REFL PLANES: 2.50 1.00 TRAN LIN: 3.50

AUG. 16,1978 A 28C -2,8,190

FREQ	MASON	MSG	MAG	MUG	GO	G1	G2	K	DELTA
4000.0	-99.99	16.00	-99.99	24.74	7.48	14.08	3.18	.05	.70
4500.0	-99.99	15.64	-99.99	19.54	6.65	9.85	3.04	.19	.67
5000.0	-99.99	15.23	-99.99	15.67	5.55	7.19	2.93	.44	.63
5500.0	-99.99	14.87	-99.99	15.44	4.78	7.62	3.04	.39	.64
6000.0	-99.99	14.55	-99.99	14.52	4.05	7.15	3.32	.42	.65
6500.0	-99.99	14.33	-99.99	14.04	3.56	7.03	3.45	.42	.65
7000.0	-99.99	14.12	-99.99	13.36	3.01	6.36	3.99	.44	.66
7500.0	-99.99	13.96	-99.99	13.72	2.63	7.17	3.91	.33	.67
8000.0	-99.99	13.80	-99.99	13.89	2.30	7.46	4.14	.25	.69
8500.0	-99.99	13.59	-99.99	12.30	1.90	5.90	4.51	.46	.67
9000.0	-99.99	13.47	-99.99	10.78	1.41	5.14	4.22	.73	.64
9500.0	-99.99	13.32	-99.99	10.53	.94	5.15	4.44	.73	.65
10000.0	-99.99	13.25	-99.99	11.38	.66	5.78	4.94	.51	.69
10500.0	-99.99	13.02	-99.99	9.48	-.40	4.66	5.22	.79	.66
11000.0	-99.99	12.98	-99.99	11.85	-.78	4.86	7.77	.18	.72
11500.0	-99.99	12.75	-99.99	15.56	-.80	6.24	10.12	-.26	.80
12000.0	-99.99	12.38	-99.99	13.78	-1.32	6.85	8.26	-.14	.79

REFL PLANES: 2.50 1.00 TRAN LIN: 3.50

2: TASK? PARAM? OUTPUT?

best gains observed from epi wafers. The S-parameter measurement results are given in Table 35 with a source-to-drain dc bias of 8 V and -2 V applied to the gate.

The second ion-implanted wafer processed, A48, also showed good S-parameter results, as given in Table 36. The maximum stable gain was 12 dB and the S_{21} gain was -2.41 dB at 12 GHz. It should be noted that for this measurement the source-to-drain dc bias was only 6 V with -2 V applied to the gate. The reason for this was that devices from wafer A48 had very low source-to-drain breakdown voltages, in the range of 6 to 8 V. This problem was also encountered with wafer A28C so that no meaningful power gain data could be obtained from either wafer. Because the implantation depth limitation did not allow the formation of a recessed gate structure, selective implantation of n^+ region in the source and drain areas was investigated as a means of improving the source-to-drain breakdown voltage. Unfortunately, to date processing problems such as contamination of the surface by the material used as the implantation mask have prevented the successful production of devices.

TABLE 36. S-PARAMETER OF AN 8-GATE FET FROM WAFER A48

A48-1 -2, 6.0, 145MA JAN 8,1979

FREQ	S11		S21		S12		S22	
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
8000.0	.833	-156.8	1.163	36.7	.052	6.1	.798	-81.0
8500.0	.809	-164.4	1.153	29.1	.053	2.9	.836	-85.1
9000.0	.791	-168.0	1.054	23.1	.051	1.9	.802	-89.4
9500.0	.824	-170.4	1.007	18.1	.050	1.6	.812	-93.6
10000.0	.787	-174.0	.951	13.4	.048	.5	.828	-95.2
10500.0	.795	-177.6	.917	9.5	.049	.7	.828	-96.7
11000.0	.814	177.7	.882	4.0	.049	-1.4	.813	-99.0
11500.0	.791	172.7	.808	-4.4	.047	-4.3	.806	-100.3
12000.0	.781	169.9	.757	-9.9	.045	-3.6	.788	-103.8

REFL PLANES: 2.50 1.70 TRAN LIN: 4.20

A48-1 -2, 6.0, 145MA JAN 8,1979

FREQ	MASON	MSG	MAG	MUG	G0	G1	G2	K	DELTA
8000.0	-99.99	13.53	-99.99	10.85	1.31	5.14	4.40	.83	.66
8500.0	-99.99	13.35	-99.99	11.07	1.24	4.61	5.21	.75	.67
9000.0	16.28	13.19	10.80	9.16	.45	4.26	4.47	1.16	.63
9500.0	-99.99	13.01	-99.99	9.68	.06	4.94	4.68	.94	.66
10000.0	16.37	12.93	10.37	8.78	-.44	4.20	5.02	1.18	.64
10500.0	17.22	12.68	10.37	8.60	-.75	4.33	5.02	1.15	.65
11000.0	16.00	12.59	9.90	8.32	-1.09	4.72	4.69	1.20	.65
11500.0	10.68	12.35	7.63	6.96	-1.85	4.26	4.56	1.65	.63
12000.0	8.44	12.24	6.38	5.89	-2.41	4.08	4.22	2.05	.61

REFL PLANES: 2.50 1.70 TRAN LIN: 4.20

2: TASK? PARAM? LIST?

Toward the end of the project it was possible to purchase some epitaxial layer wafers from an outside vendor. Wafer 20392C had an undoped buffer layer and an n layer thick enough for processing by the self-aligned gate technique. Since there was no n^+ contact layer, an AuGe/Ni metallization was used to produce the ohmic contacts. At 12 GHz the usable gain (MAG) was 5.26 dB and the S_{21} was

TABLE 37. A. SMALL-SIGNAL GAIN OF AN 8-GATE FET. THE MAG IS 5.26 dB AT 12 GHz. B. S-PARAMETER OF AN 8-GATE FET

20392C-4 -2, 8.0, 305MA NOV 6, 1978

FREQ	MASON	MSG	MAG	MUG	GO	G1	G2	K	DELTA
4000.0	33.50	12.95	-99.99	13.13	6.18	6.50	.45	.36	.15
4500.0	-99.99	12.55	-99.99	13.24	5.44	7.32	.47	.28	.17
5000.0	-99.99	12.14	-99.99	12.09	4.54	7.04	.51	.34	.18
5500.0	-99.99	11.87	-99.99	11.27	3.95	6.73	.60	.39	.21
6000.0	20.33	11.56	-99.99	9.76	3.14	5.97	.65	.57	.22
6500.0	15.36	11.22	-99.99	8.52	2.39	5.36	.78	.72	.25
7000.0	13.58	10.98	-99.99	7.71	1.84	4.97	.90	.84	.27
7500.0	14.86	10.75	-99.99	7.58	1.38	5.26	.94	.80	.29
8000.0	13.94	10.58	-99.99	7.08	.91	5.07	1.10	.87	.31
8500.0	11.79	10.46	9.80	6.42	.46	4.77	1.19	1.01	.33
9000.0	9.95	10.31	7.60	5.65	-.05	4.43	1.27	1.20	.34
9500.0	8.43	10.13	6.45	4.95	-.61	4.16	1.40	1.38	.35
10000.0	7.82	10.00	5.88	4.54	-1.02	4.08	1.48	1.48	.36
10500.0	8.65	9.96	6.32	4.75	-1.11	4.30	1.56	1.37	.38
11000.0	12.29	9.84	8.18	5.47	-.83	4.68	1.62	1.07	.39
11500.0	12.08	9.86	7.87	5.71	-.77	4.98	1.50	1.11	.41
12000.0	7.42	9.74	5.26	4.36	-2.25	5.17	1.43	1.58	.42

REFL PLANES: 2.50 1.70 TRAN LIN: 4.20

2: TASK? PARAM? LIST?

MSC 20392C-4 -2, 8.0, 305MA NOV 6, 1978

FREQ	S11		S21		S12		S22	
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
4000.0	.881	-135.1	2.037	78.2	.103	8.8	.312	-104.4
4500.0	.903	-140.7	1.871	71.0	.104	5.1	.321	-110.0
5000.0	.896	-148.0	1.687	63.3	.103	-.6	.334	-117.7
5500.0	.887	-150.9	1.575	57.5	.102	-4.1	.359	-121.8
6000.0	.864	-154.4	1.436	52.1	.100	-7.6	.372	-125.7
6500.0	.842	-156.9	1.317	46.9	.099	-10.2	.405	-130.4
7000.0	.826	-158.8	1.235	41.6	.099	-12.4	.433	-134.7
7500.0	.838	-160.7	1.172	37.0	.099	-14.2	.441	-138.9
8000.0	.830	-162.6	1.111	32.4	.097	-16.3	.472	-142.8
8500.0	.816	-165.4	1.054	27.5	.095	-19.1	.489	-146.5
9000.0	.799	-170.4	.994	21.9	.093	-21.4	.504	-148.5
9500.0	.785	-173.4	.932	18.6	.090	-23.7	.524	-150.8
10000.0	.781	-174.7	.889	14.5	.089	-24.5	.537	-154.0
10500.0	.793	-174.6	.880	11.9	.089	-25.0	.549	-156.9
11000.0	.812	-176.4	.909	6.8	.094	-26.6	.558	-161.3
11500.0	.826	-177.6	.915	-3.6	.095	-34.7	.541	-162.8
12000.0	.834	178.5	.772	-10.2	.082	-38.8	.530	-161.3

REFL PLANES: 2.50 1.70 TRAN LIN: 4.20

-2.25 dB. These results are comparable to those obtained from the better wafers produced at RCA. The S-parameter results are given in Table 37. The power gain of devices from wafer 20392C were measured at 10 and 15 GHz. Tables 38 and 39

TABLE 38. P_{in}-P_{out} CHARACTERISTICS OF AN 8-GATE FET FROM WAFER 20392-C at 10 GHz

20392-C-4 8-Gate FET

V_D = 8 V, V_G = -1.5 V, f = 10 GHz

P_{in}(mW)	P_{out}(mW)	G(dB)	I_D(mA)	P_{out}-P_{in}(mW)	η_{PA}(%)
50	258.7	7.4	334		
100	485.1	7.1	342		
150	646.8	6.6	334		
200	770	6.1	316		
237.5	847	5.5	305	609.5	25.0
300	908.6	5.0	296	623.6	26.3

TABLE 39. P_{in}-P_{out} CHARACTERISTICS OF AN 8-GATE FET FROM WAFER 20392-C at 10 GHz

20392-C-6 8-Gate FET

V_D = 8 V, V_G = -1.5 V, f = 10 GHz

P_{in}(mW)	P_{out}(mW)	G(dB)	I_D(mA)	P_{out}-P_{in}(mW)	η_{PA}(%)
20	89.7	6.5	180		
50	208.8	6.2	184		
100	389.7	5.9	194		
150	514.7	5.4	198		
200	595.6	4.7	189	395.6	26
250	647.1	4.1	177	397	28

give the power gain results at 10 GHz for devices 20392-C-4 and 20392-C-6, respectively. Power gain measured at 15 GHz for these two devices is shown in Tables 40 and 41.

The power performance of the best devices produced during this contract period is summarized in Table 42. The highest output power at 15 GHz achieved in this program was 1.05 W from wafer D147. The best efficiency at 15 GHz was

TABLE 40. P_{in}-P_{out} CHARACTERISTICS OF AN 8-GATE FET FROM WAFER 20392-C at 15 GHz

20392-C-4 8-Gate FET

V_D = 8 V, I_{DSSO} = 490 mA, V_G = -1.5 V, f = 15 GHz

P_{in}(mW)	P_{out}(mW)	G(dB)	I_D(mA)	P_{out}-P_{in}(mW)	η_{PA}(%)
45	143.55	5.0	324		
90	275.5	4.9	328		
180	449.5	4.0	324		
225	493	3.4	319	268	10.5
V_D = 9 V, V_G = -1.5V, f = 15 GHz					
45	166.75	5.7	321		
90	297.25	5.2	326		
135	423.4	5.0	330		
180	507.5	4.5	328	327.5	11.1
225	565.5	4.0	324	340.5	11.7

TABLE 41. P_{in}-P_{out} CHARACTERISTICS OF AN 8-GATE FET FROM WAFER 20392-C at 15 GHz

20392-C-6 8-Gate FET

V_D = 9 V, V_G = -1.5 V, f = 15 GHz

P_{in}(mW)	P_{out}(mW)	G(dB)	I_D(mA)	P_{out}-P_{in}(mW)	η_{PA}(%)
45	129.05	4.6	170		
90	234.9	4.2	172		
135	326.25	3.8	172		
180	406	3.5	172	226.0	14.6

19% with 0.74-W output power (Table 42). It is believed that the program goal of 2-W output power can be realized with a proper combination of good n^+ layer and buffer layer.

TABLE 42. SUMMARY OF GaAs POWER FET PERFORMANCE

Wafer No.	FET Type	Frequency (GHz)	Power Gain (dB)	Output Power (W)	Power-Added Efficiency (%)
A105	18 Gate	10	3.9	1.26	11.8
C182	8 Gate	15	3.1	0.743	19
B995	18 Gate	15	1.5	0.556	3.8
D147	18 Gate	15	2.0	1.05	8.6
D169	8 Gate	10	4.4	0.476	11.5
D319	18 Gate	15	2.14	0.88	6.7
C521	8 Gate	15	3.2	0.66	10.7
20392-C	8 Gate	15	3.5	0.41	14.6

SECTION V

AMPLIFIER DEVELOPMENT

A. MSC88102 (8-GATE) SINGLE-STAGE AMPLIFIER

With lumped-element carrier matching and large-signal characterization techniques, it was shown that at 15 GHz, 8-gate, 1200-μm width devices are capable of 20% power-added efficiency with an output power of 0.5 W and 4.0-dB gain. This transistor type was characterized over the 13- to 15-GHz band, and a design using lumped and distributed matching networks was implemented. Only time prevented the realization of this amplifier stage completely in a lumped-element format.

Figure 92 is a photograph of the 8-gate amplifier design. This stage occupies a volume of 5/8x3/8x5/8 $in.^3$ excluding the box wall thicknesses. The distributed transmission line networks are fabricated on low loss quartz substrates. The width of the amplifier is calculated to prevent only TEM modes from propagating by essentially forming a waveguide below cutoff with the box and its cover (not shown). The device in this picture has lumped-element matching only on the gate side of the device. With complete lumped-element matching, this amplifier may be reduced in size down to a volume of 0.125x 0.125x0.5 $in.^3$.

The performance of an 8-gate amplifier stage over the band of interest is shown in Fig. 93. For this stage with 0.225 W of input power, the gain is 3.3 ± 0.1 dB over the 14.4- to 15.4-GHz band of interest. The output power and minimum-efficiency corresponding to this input power are 0.48 W and 15%, respectively. It should be noted that the best 15-GHz results for this device type are 4.0-dB gain and 20% efficiency. The slightly lower amplifier efficiency may be attributed to external losses in the matching networks and operation of the device over the full band. We believe that by realizing this amplifier stage in a lumped-element format, in addition to the amplifier size reduction realized, there will also be a slight improvement in performance due to decreased circuit losses.

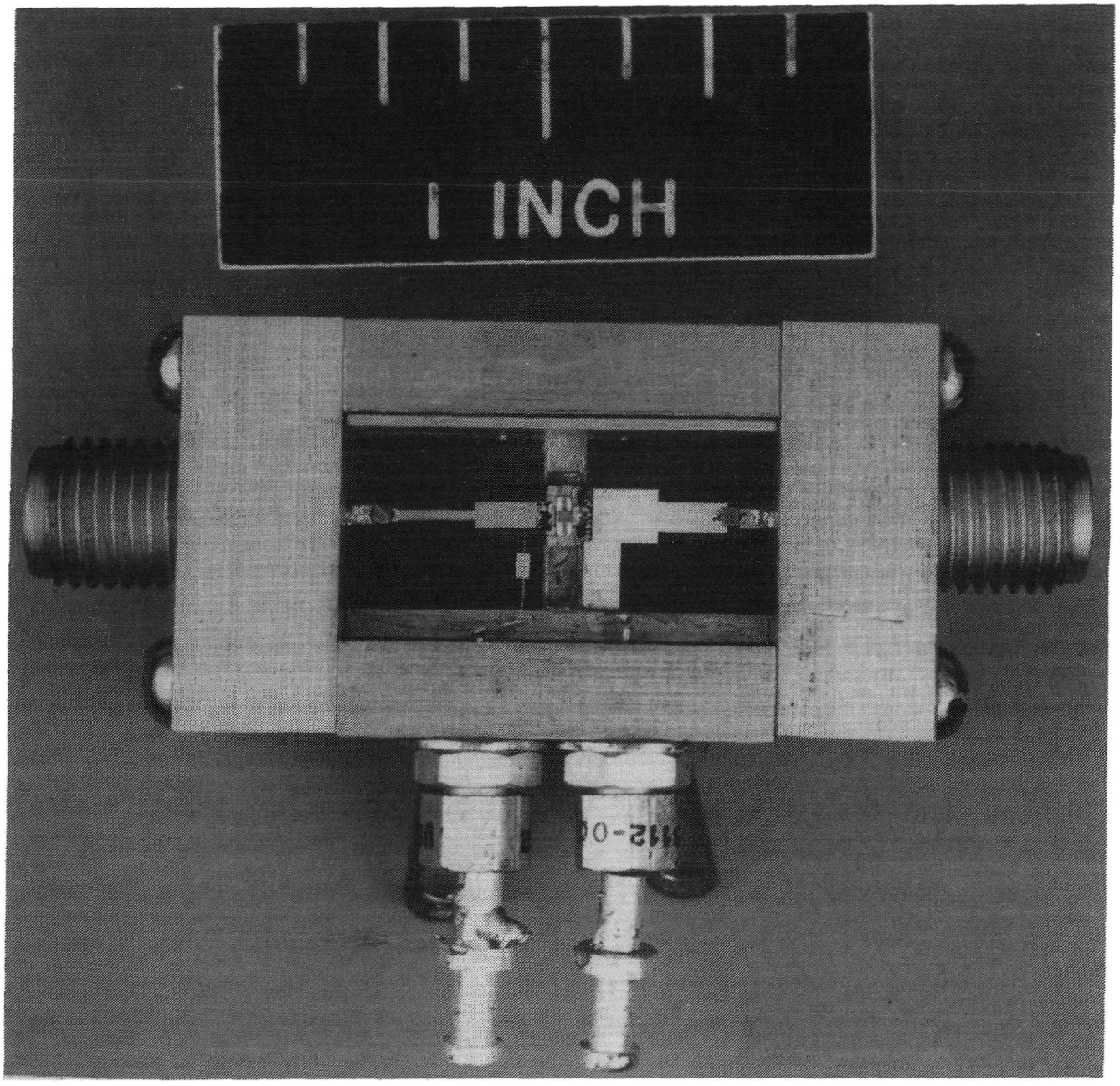


Figure 92. 8-gate single-stage amplifier.

B. CHIP LEVEL COMBINING OF MSC88102 DEVICES

In order to achieve high-power output at 15 GHz, two 8-gate devices were combined and matched on the device carriers using the newly developed lumped-element format. We used this approach because the device proposed for this stage is still in development and was not available when required.

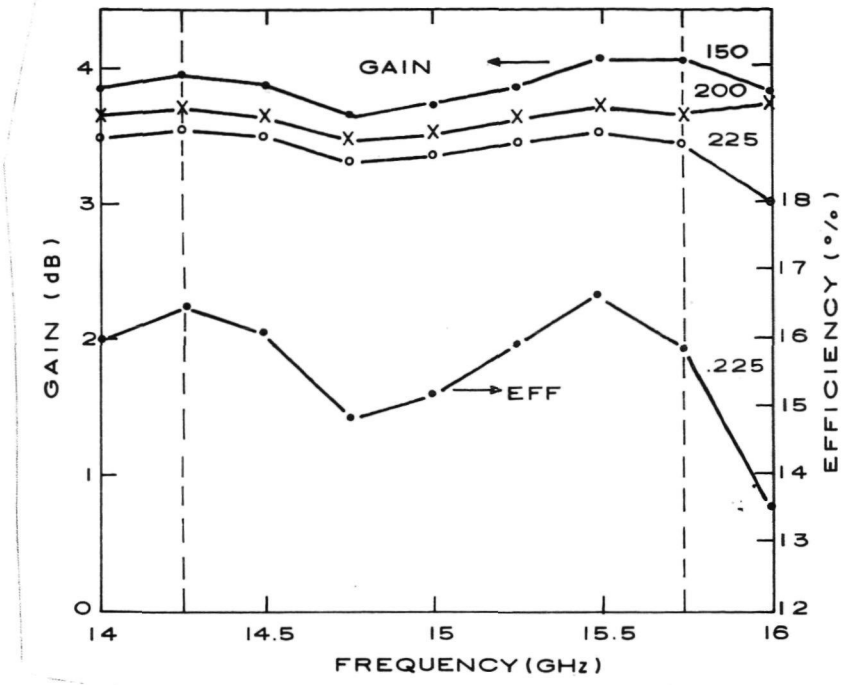
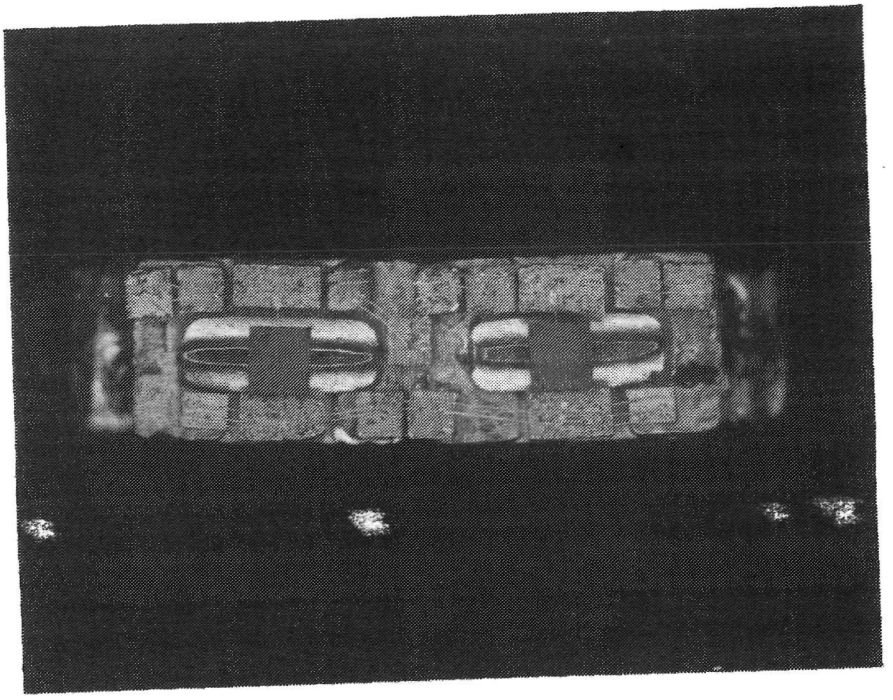
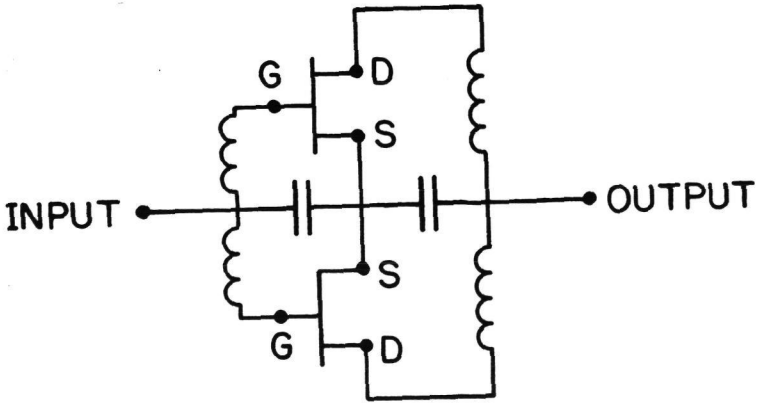


Figure 93. 8-gate amplifier gain and efficiency vs frequency.

Figure 94(a) is a photograph of two 8-gate devices which were matched on their own carriers and then combined. This total volume of the amplifier stage is 0.060x0.120x0.030 $in.^3$ and weighs less than 4 grams. In this combiner, simple single-section, low-pass networks are used which are schematically shown in Fig. 94(b). Figure 95 shows the gain efficiency and gain versus frequency with input power of 0.3 and 0.4 W, respectively. The gain is approximately 3 dB over the band 15 ± 0.5 GHz. The best efficiency over this bandwidth is 9.9% with 0.8-W output power at 14.7 GHz. The gain efficiency and bandwidth can definitely be optimized further under large signal conditions. The efficiency of one 8-gate device over the acceptable band has been shown in the previous section to be a minimum of 15%. Thus, the poor combining efficiency is due either to excessive circuit losses or poor large signal matching. We feel that excessive loss is the problem, and with further refinements, the combining efficiency will definitely be improved.



(a)



(b)

Figure 94. Stage 3 realization using two 8-gate devices, carrier matched and combined. (a) Photograph; (b) equivalent circuit.

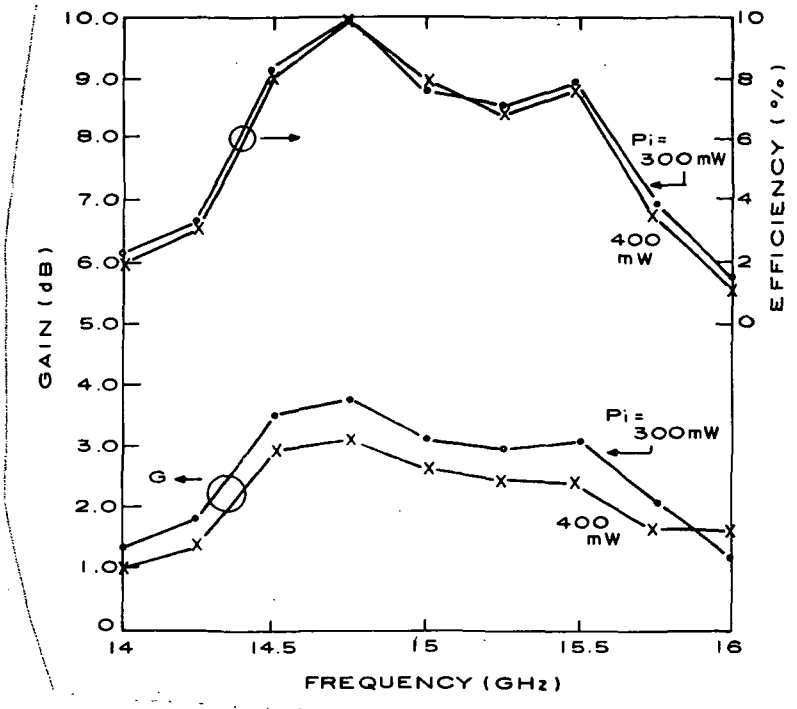


Figure 95. Efficiency and gain vs frequency of stage B.

SECTION VI

SUMMARY OF RESULTS

This report describes the work performed during a 20-month research program to develop GaAs FETs and associated circuitry for medium-power Ku-band amplifiers. The program comprises materials research, device technology development, and amplifier studies. The significant results obtained in each of these areas are summarized below.

A. MATERIALS RESEARCH

The major materials effort in this program was the growth of n^+-n-SI GaAs wafers for the device development effort. During the program period, device-quality epitaxial material was produced by three $AsH_3/Ga/HCl/H_2$ (hydride) reactors and one $AsCl_3$ reactor. These reactors were designed, fabricated, and debugged under RCA sponsorship. The technology for the growth of Cr-doped buffer layers in the hydride system was refined. The surface morphology of Cr-doped buffer layers was excellent. The voltage breakdown of Cr-doped layers was in excess of 1500 V, and the resistivity was of the order of 10^7 ohm-cm. Undoped buffer layers were grown using the two-bubbler $AsCl_3$ system, and their resistivity was estimated to be about 10^5 ohm-cm.

Device quality n-SI GaAs wafers were also produced by ion implantation in the 50- to 250-keV energy range using ^{28}Si ions. A method was developed for annealing implanted wafers without encapsulation under arsenic overpressure. This procedure has been very successful, and implanted wafers with excellent surface morphology have been obtained.

B. DEVICE TECHNOLOGY

FET structures with gate widths of 1200, 2400, and 3150 μm with design powers of 0.75, 1.5, and 2.0 W, respectively, are under development. Two device fabrication techniques were used for device fabrication during this project. The bulk of the devices were fabricated by a previously developed self-aligned gate process. During the project, an aligned-gate fabrication process was developed. A novel feature of this process is the use of a moat etch plus anodic thinning to compensate for epitaxial layer thickness variations

by automatically thinning the gate channels to the pinch-off thickness while leaving a layer of n^+ material in the source and drain regions. A double layer photoresist technique was developed to allow clean lift-off of thick gate metallization. The thick bottom photoresist layer allows clean lift-off of the gate metallization and acts to smooth out surface features to allow definition of 1-μm gate lengths in the top photoresist layer.

The highest output power at 15 GHz achieved in this program was 1.05 W. The best efficiency at 15 GHz was 19% with 0.74-W output power.

The key features of our FET device technology are: (a) use of refractory, Au-based metallization for the source, drain, and gate contacts, and (b) flip-chip mounting. The use of refractory Au-based metallization, particularly for the Schottky-barrier gate contact, results in higher device reliability. Unlike low-noise FETs, power FETs operate at high channel temperature, large rf voltage swings, and high rf gate current in both the forward conduction and reverse breakdown regions. These factors enhance intermetallic diffusion and electromigration, which are common failure modes. Intermetallic diffusion and electromigration are strongly dependent on the gate metallization and are particulary severe for Al-based gates. The operating-channel temperature depends substantially on the design and packaging of the FET. The flip-chip mounted design pioneered by RCA under USAF Avionics Laboratory sponsorship (Contract No. F33615-73-C-1042) leads to both low thermal resistance and low parasitic source inductance. Measurements show that the temperature rise in a flip-chip bonded FET capable of 1 W of rf output is only about 60 to 65°C. As as result of these two factors, RCA power FETs have potential for high reliability. Preliminary accelerated life test data on RCA FETs indicates an MTBF of at least 1.4×10^6 h, based on a conservative estimate of 1-eV activation energy and 130°C channel temperature.

C. AMPLIFIER DEVELOPMENT

In this project a single-stage amplifier was developed using an 8-gate, 1200-μm width device to give a gain of 3.3 ± 0.1 dB over the 14.4- to 15.4-GHz band with an output power of 0.48 W and 15% minimum efficiency with 0.255 W of input power. With two 8-gate devices combined and matched on the device carrier, using a newly developed lumped-element format, a gain of 3 dB was attained over the 14.5- to 15.5-GHz band with a maximum efficiency of 9.9% for an output power of 0.8 W.

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